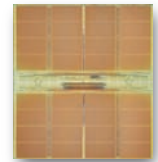




XDR™ DRAM

ELPIDA

Industry demand for memory bandwidth in next-generation digital consumer electronics, such as high-definition digital television, home servers and high-end 3-D graphics applications, is growing rapidly as more content becomes available and as processor performance becomes more robust.



Elpida Memory has developed ultra-high-speed 512Mb XDR DRAM based on the XDR memory interface technology developed by Rambus Inc., and these devices are currently in volume production.

Our 512Mb XDR DRAM devices provide an industry-leading data transfer rate of 6.4GB/s, 8.0GB/s, 9.6GB/s within a single device, through 3.2Gbps, 4.0Gbps, 4.8Gbps ultra-high-speed data transfer operation and x16-bit I/O configuration. This performance is 4 to 6 times the peak bandwidth of the latest DDR2 standard memory adopted in PC applications.



Features of XDR DRAM

Highest pin bandwidth

- 3.2Gbps, 4.0Gbps, 4.8Gbps Octal Data Rate (ODR) signaling
 - 3.2GHz, 4.0GHz, 4.8GHz data rate, octuple the system clock transfer rate of 400MHz, 500MHz, 600MHz
- Bi-directional differential RSL (DRSL)
 - Flexible read / write bandwidth allocation
 - Minimum pin count
- On-chip termination
 - Reduced system cost and routing complexity

Highest sustained bandwidth per DRAM device

- 6.4GB/s, 8.0GB/s, 9.6GB/s peak data transfer rate
- 8 banks: Bank-interleaved transactions at full bandwidth
- Dynamic request scheduling
- Early-read-after-write support for maximum efficiency
- Zero overhead refresh

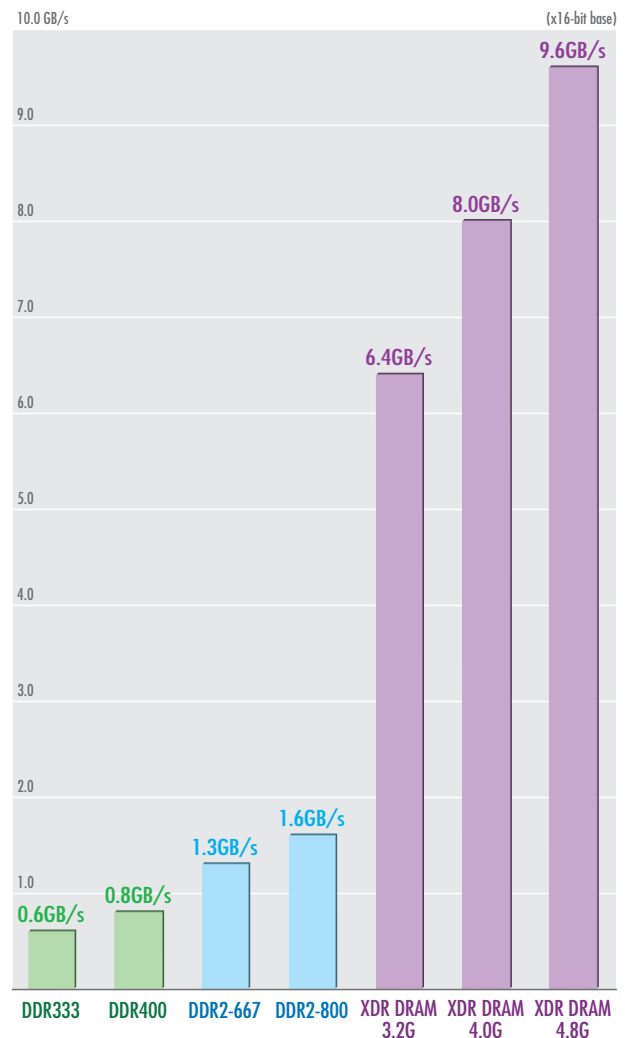
Low power

- 1.8V VDD
- Small-swing I/O signaling (DRSL) (200mV)
- Power-down self-refresh support

Package

- 104-ball FBGA
 - 15.18mm x 14.56mm
- Ball-pitch
 - 1.27mm / 0.8mm

DRAM Bandwidth





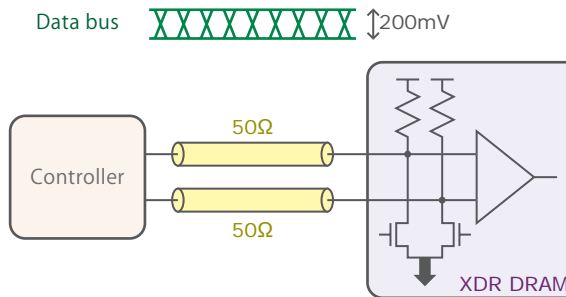
XDR DRAM

ELPIDA

XDR Memory Interface

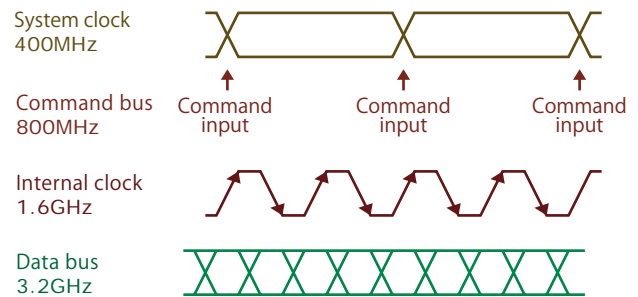
DRSL (Differential Rambus Signaling Levels)

- Bi-directional Differential Rambus Signaling Levels
- 200mV ultra-low swing signal
- On-chip termination
- Point-to-point data interconnect for fastest possible flight time



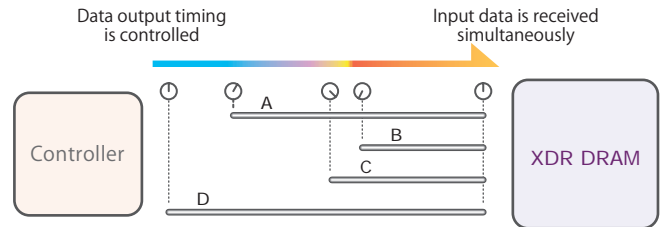
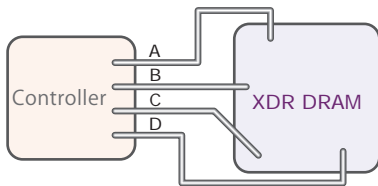
ODR (Octal Data Rate)

- 1.6GHz internal clock is generated from 400MHz clock input
- 3.2GHz data rate is enabled by referencing both edges of the internal clock
- Eight bits of data per clock



FlexPhase™

- Controlling the data output timing for each DQ pin reduces skew at destination (XDR DRAM)
- Simplifies PCB design by eliminating data trace length matching



Memory Solution for Digital TV in 2010

Required MB/system & BW (GB/s)	512Mb XDR (x16 mode)	256Mb DDR2 (x16)	512Mb DDR3-1333 (x16)	256-512Mb GDDR3-1600 (x32)
Low end 32MB/system 5GB/s	ASIC ↔ 312GHz XDR x16 bus, 6.4GB/s	ASIC ↔ DDR2-667 x64 bus, 5.2GB/s	ASIC ↔ DDR3-1333 x32 bus, 5.4GB/s	ASIC ↔ 1256Mb GDDR3-1600 x32 bus, 6.4GB/s
Mid range 64MB/system 8GB/s	ASIC ↔ 410GHz XDR x16 bus, 8.0GB/s	ASIC ↔ DDR2-1066 x64 bus, 8.4GB/s	ASIC ↔ DDR3-1333 x64 bus, 10.8GB/s	ASIC ↔ 256Mb GDDR3-1600 x64 bus, 12.8GB/s
High end 128MB/system 12GB/s	ASIC ↔ 3.2GHz XDR x32 bus, 12.8GB/s	ASIC ↔ DDR2-800 x128 bus, 12.8GB/s	ASIC ↔ DDR3-1333 x128 bus, 21.6GB/s	ASIC ↔ 512Mb GDDR3-1600 x64 bus, 12.8GB/s

XDR realizes necessary band width and MB/system with few component count, thus enabling low cost solution.