

FEATURE COMPARISON OF DDR2 SDRAM, DDR SDRAM and SDRAM

CAUTION

This document shows differences between DDR2 SDRAM, DDR SDRAM and SDRAM.

For details about the functions and specifications, refer to the corresponding data sheet or user's manual.

Differences in Functions and Specifications

Items	DDR2 SDRAM	DDR SDRAM	SDRAM
Clock frequency	200/266/333/400MHz	100/133/166/200MHz	100/133/166MHz
Transfer data rate	400/533/667/800Mbps	200/266/333/400Mbps	100/133/166MHz
I/O width	×4/×8/×16	×4/×8/×16/×32	×16/×32
Prefetch bit width	4bits	2bits	1bit
Clock input	Differential clock	Differential clock	Single clock
Burst length	4, 8	2, 4, 8	1, 2, 4, 8, full page
Data strobe	Differential data strobe	Single data strobe	Unsupported
Supply voltage	1.8V	2.5V	3.3V/2.5V
Interface	SSTL_1.8	SSTL_2	LVTTTL
/CAS latency (CL)	3, 4, 5 clock	2, 2.5, 3 clock	2, 3 clock
Read latency	AL+CL	CL	CL
Write latency	(AL+CL)-1	1	0
Additive latency (AL)	0, 1, 2, 3, 4clock	Unsupported	Unsupported
Off-chip driver (OCD)	Support	Unsupported	Unsupported
On die termination (ODT)	Support	Unsupported	Unsupported
Component package	FBGA	TSOP(II)/FBGA/LQFP	TSOP(II)/FBGA
Lead-free	Support	Support	Support

The information in this document is current as January, 2005. The information is subject to change without notice.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

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