

New Function of DDR2 SDRAM On Die Termination (ODT)

CAUTION

This document describes On Die Termination (ODT), a new function that has been added to DDR2 SDRAM.

For details about the functions, refer to the corresponding data sheet or user's manual.

In addition, operation and the numerical value that appear in this manual show the example of reference.

1. Signal Reflection

A ball that is thrown against a wall will bounce back. Similarly, electrical signals are reflected back when they reach the end of a transmission path. Electrical signals also can be reflected at points where impedance differs, such as at bus and DRAM connection points.

Signal reflection causes noise, which lowers signal quality. In a high-speed data transfer system, high-quality signals are required and even a slight amount of noise can be a major problem.

2. Motherboard Termination

Motherboard termination is a termination method that reduces signal reflection by attaching a resistor (termination resistance) with a suitable resistance value at the end of each transmission path. However, this method does not reduce signal reflection adequately in the operating frequency range used by DDR2 SDRAM. Also, adding termination resistors to the motherboard increases the component count and tends to raise costs.

2.1 Signal reflection when using motherboard termination

As mentioned above, motherboard termination may not be able to reduce signal reflection adequately. If there are several DRAMs on the same bus, such as is shown in Figure 2-1, DRAM currently being accessed is affected by reflected signals from other DRAM.

Thus, to ensure high signal quality required in a high-speed data transfer system, a processing technology is needed to control signal reflection with greater precision than is possible with motherboard termination.

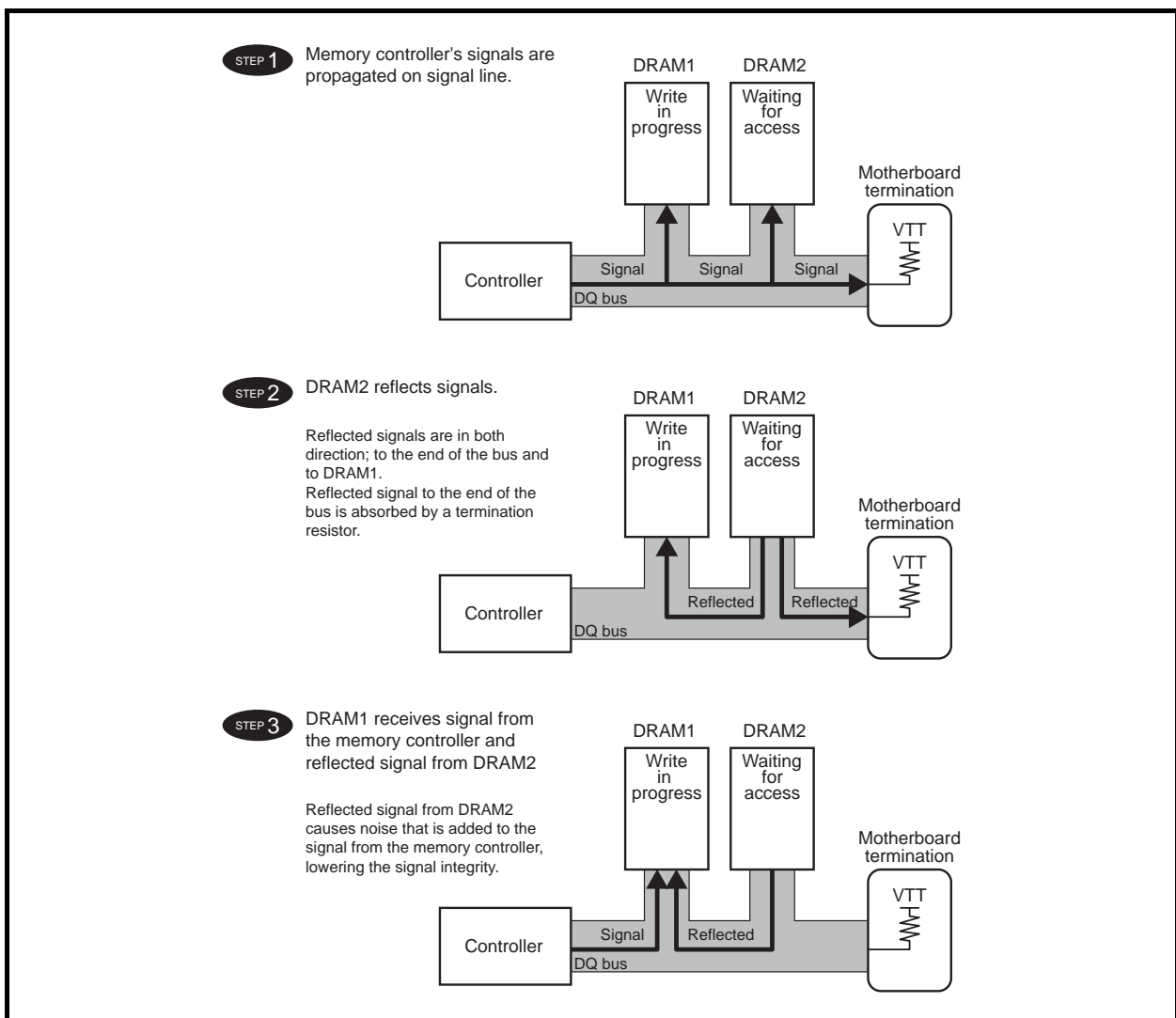


Figure 2-1 Signal Reflection when Using Motherboard Termination

3. Overview of ODT

When using ODT, the on-die termination resistance for each DRAM can be switched ON and OFF.

Accordingly, even when several DRAMs exist on the same bus, signals transmitted to the DRAM can be terminated.

As a result, DRAM currently being accessed is less likely to be affected by reflected signals from other DRAM.

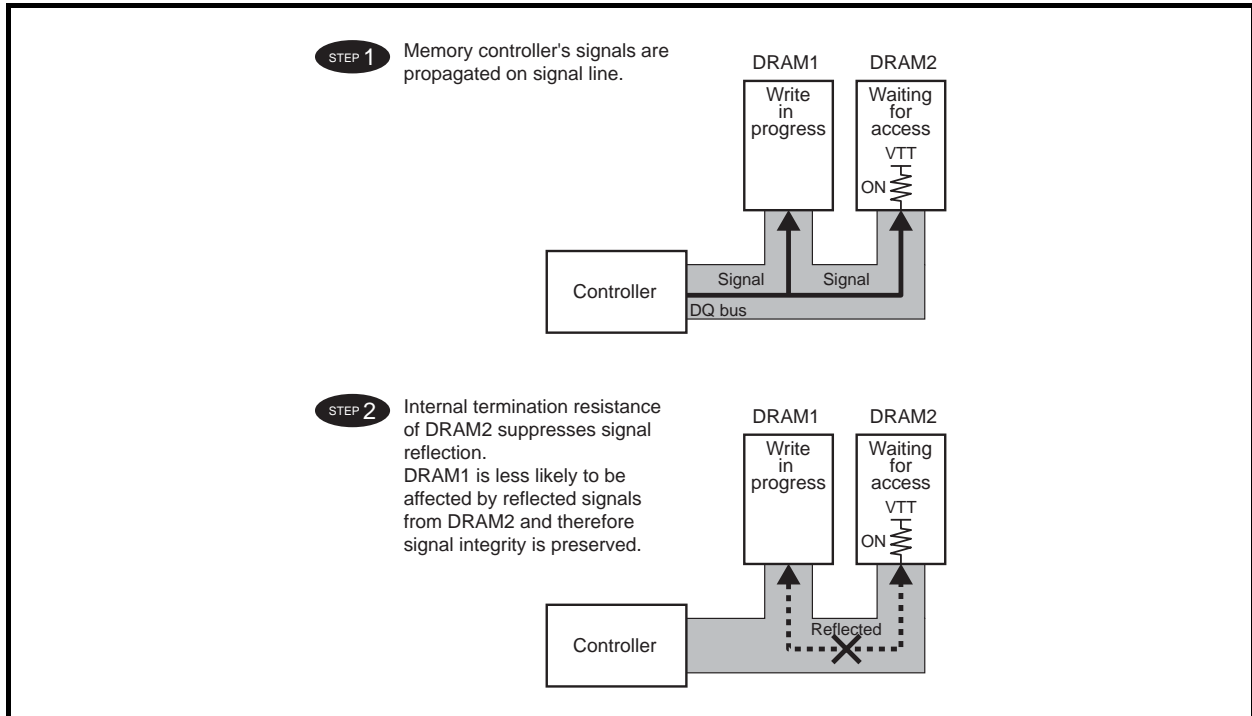


Figure 3-1 ODT and Reflected Signals

3.1 ODT features

DDR2 SDRAM embeds the termination resistors that used to be placed on the motherboard. The DRAM controller can use

ODT to set the termination resistance simultaneously to each pin (DQ, DQS, /DQS, RDQS, and /RDQS) ON and OFF.

The impedance value of the termination resistors can be selected as "ODT not selected", "ODT selected (50Ω)", "ODT selected (75Ω)", or "ODT selected (150Ω)". The value to be selected is set in advance via EMRS (1), (Extended Mode Registers Set (1)).

3.2 Advantages of ODT

DDR2 SDRAM contains termination resistors that were previously mounted on the motherboard, thereby reducing the number of parts on the motherboard. This also eliminates some of the wiring on the motherboard, which facilitates system design.

3.3 Structure of ODT

DDR2 SDRAM can use the ODT control pin to set the termination resistance simultaneously to each pin (DQ, DQS, /DQS, RDQS, and /RDQS) ON and OFF. The termination resistor's impedance value is set in advance via EMRS (1) (Extended Mode Registers Set (1)).

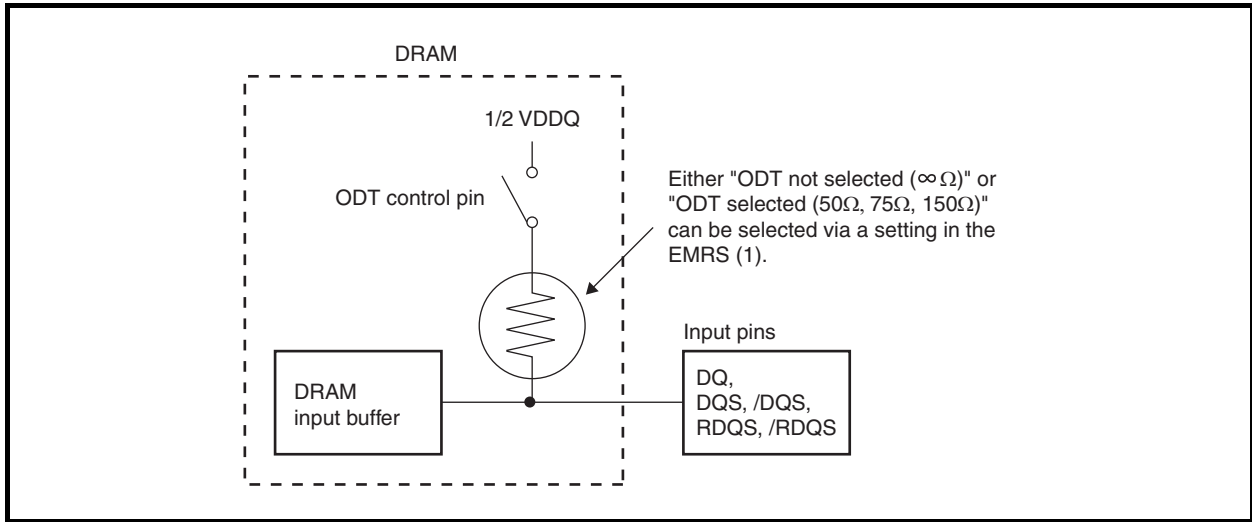


Figure 3-2 Structure of ODT

4. Setting of ODT Impedance Value

The ODT impedance value is set via EMRS (1) (Extended Mode Registers Set (1)).

Use two bits (A6 and A2) to select "ODT not selected", "ODT selected (50Ω)", "ODT selected (75Ω)", or "ODT selected (150Ω)". Once the ODT impedance value is set, the setting is retained until another setting is entered or the power is turned off.

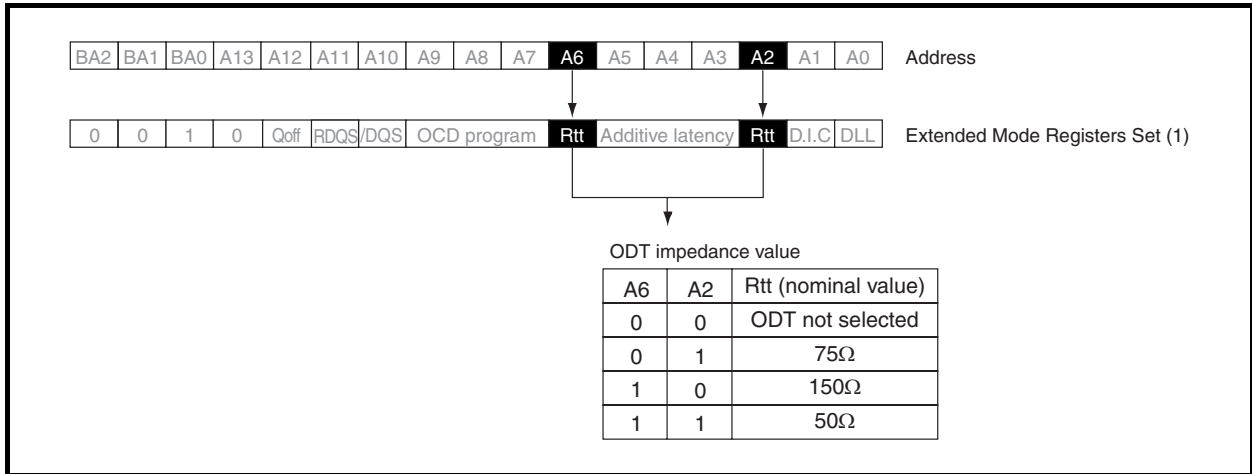


Figure 4-1 ODT Impedance Value Settings via Extended Mode Registers Set (1)

5. ODT ON/OFF Timing

The ODT settings are controlled based on the input level of the ODT control pin. The standard value of ODT timing varies between power-down mode and other modes (such as active mode or standby mode).

5.1 ODT ON/OFF timing for power-down mode

Figure 5-1 shows the ODT ON/OFF timing for power-down mode.

When ODT is set to ON (ODT control pin input is at high level) during power-down mode, the ODT turn-on delay time (t_{AONPD}) elapses, then the internal termination resistor (R_{tt}) is set to ON.

When ODT is set to OFF (ODT control pin input is at low level) during power-down mode, the ODT turn-off delay time (t_{AOFPD}) elapses, then the internal termination resistor (R_{tt}) is set to OFF.

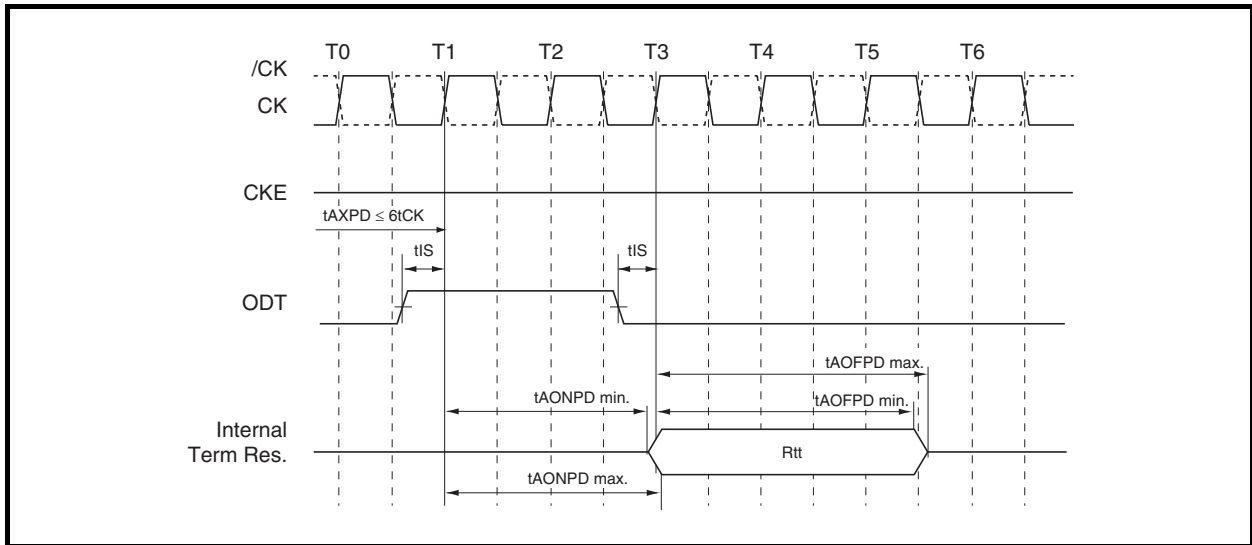


Figure 5-1 ODT ON/OFF Timing for Power-down Mode

5.2 ODT ON/OFF timing for active mode and standby mode

Figure 5-2 shows the ODT ON/OFF timing for active mode and standby mode.

When ODT is set to ON (ODT control pin input is at high level) during either standby mode or active mode, the ODT turn-on delay time (t_{AOND}) elapses, then the internal termination resistor (R_{tt}) is set to ON.

When ODT is set to OFF (ODT control pin input is at low level) during either standby mode or active mode, the ODT turn-off delay time (t_{AOFD}) elapses, then the internal termination resistor (R_{tt}) is set to OFF.

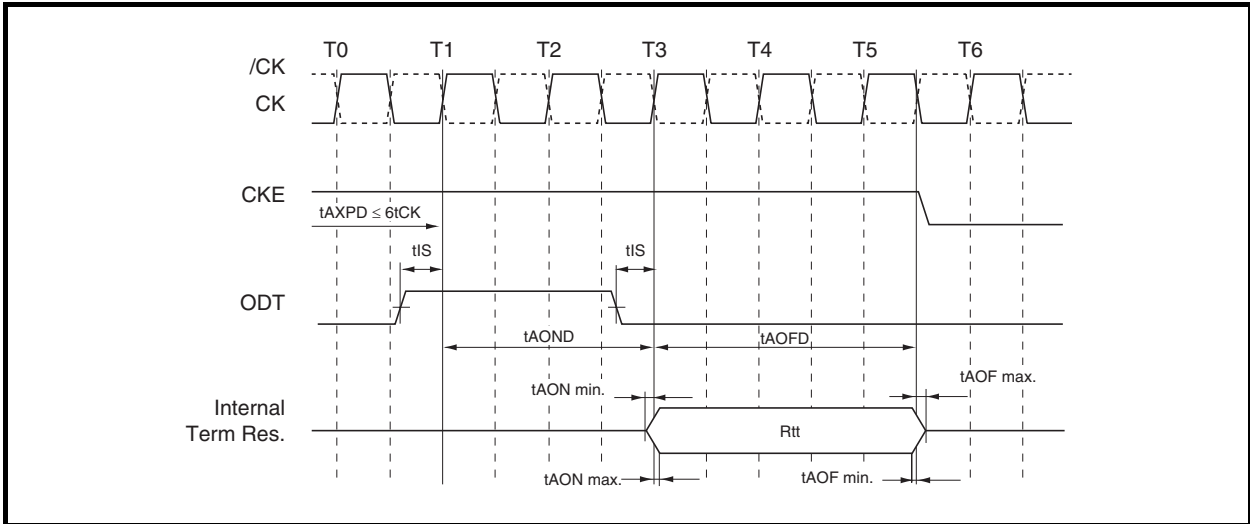


Figure 5-2 ODT ON/OFF Timing for Active Mode and Standby Mode

5.3 ODT ON timing at entering power-down mode

Figure 5-3 shows the timing when ODT is set to ON while entering power-down mode.

The turn-on delay time must elapse before ODT is turned ON. The timing differs depending on whether or not this delay time has elapsed when power-down mode is entered. If the delay time has not elapsed when power-down mode is entered, the ODT turn-on delay time will be longer than normal.

When power-down mode is entered after the ODT turn-on delay time has elapsed, DRAM is set to active mode or standby mode at the same time as power-down mode is entered.

If power-down mode is entered before ODT turn-on delay time has elapsed, the DRAM is set to power-down mode.

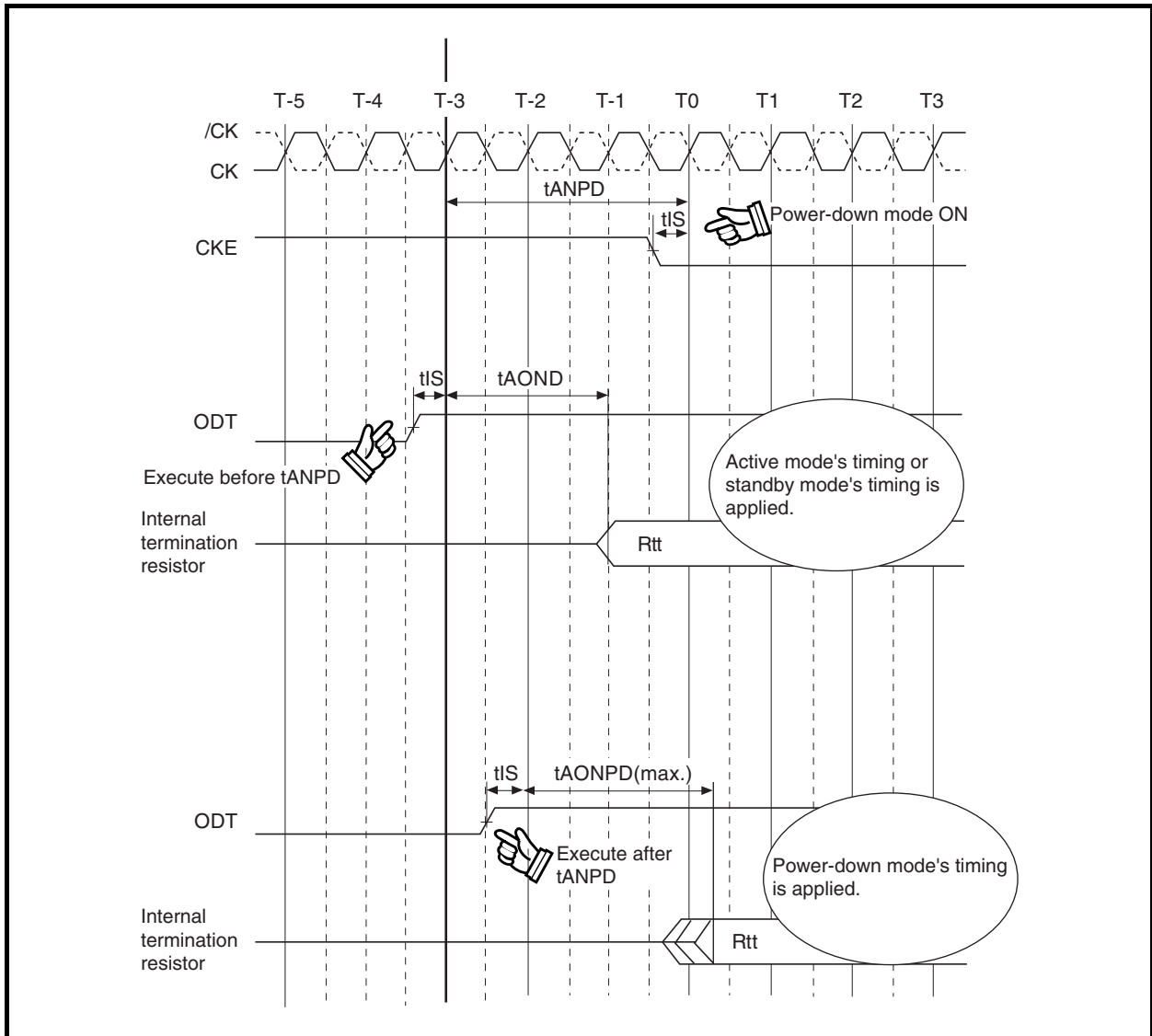


Figure 5-3 ODT ON Timing at Entering Power-down Mode

5.4 ODT OFF timing at entering power-down mode

Figure 5-4 shows the timing when ODT is set to OFF while entering power-down mode.

The turn-off delay time must elapse before ODT is turned OFF. The timing differs depending on whether or not this delay time has elapsed when power-down mode is entered. If the delay time has not elapsed when power-down mode is entered, the ODT turn-off delay time will be longer than normal.

When power-down mode is entered after the ODT turn-off delay time has elapsed, the DRAM is set to active mode or standby mode at the same time as power-down mode is entered.

If power-down mode is entered before ODT turn-off delay time has elapsed, the DRAM is set to power-down mode.

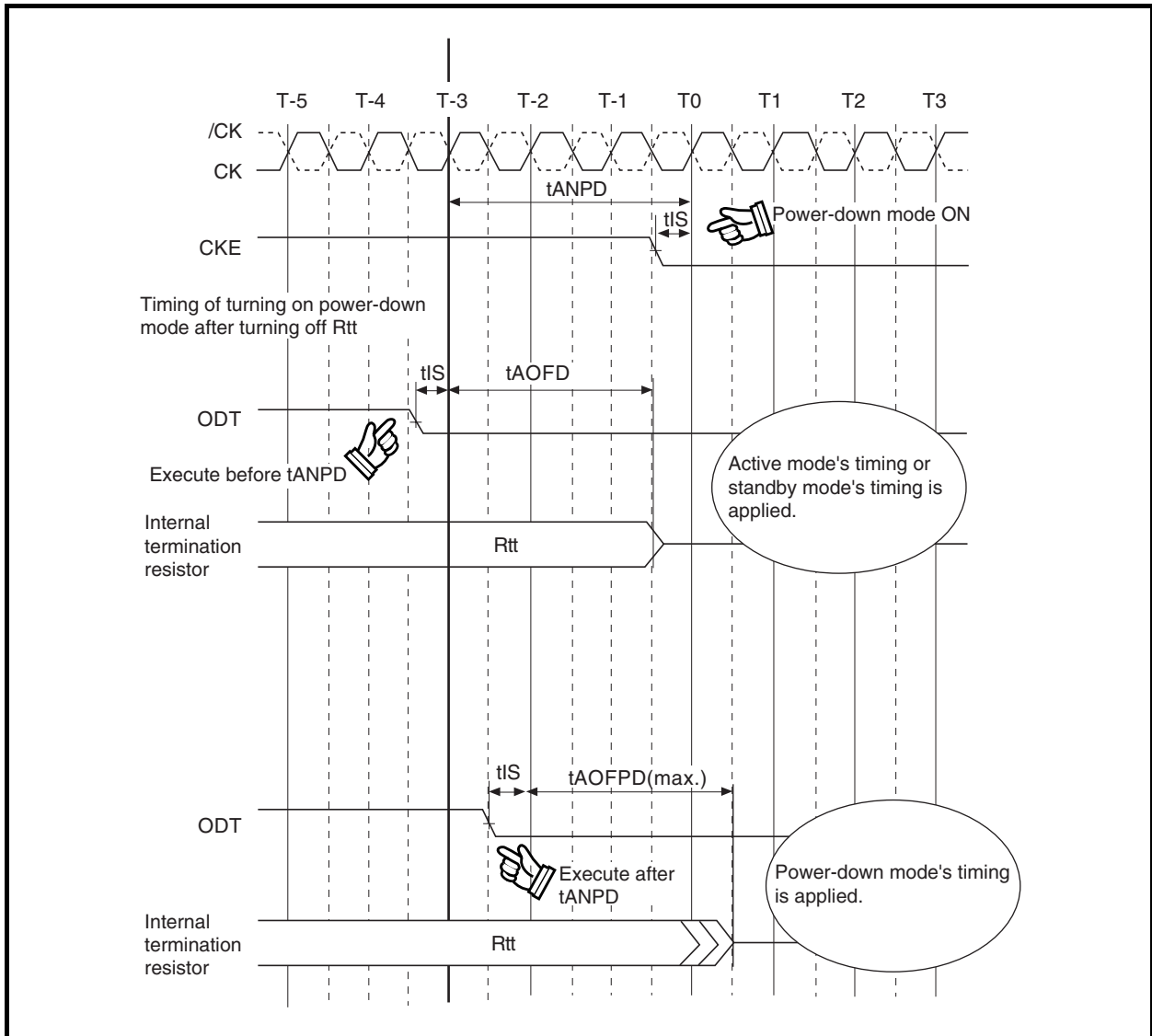


Figure 5-4 ODT OFF Timing at Entering Power-down Mode

5.5 ODT ON timing at exiting power-down mode

Figure 5-5 shows the timing when ODT is set to ON while exiting power-down mode. The exit delay time (t_{AXPD}) must elapse before exiting power-down mode. The timing of ODT turn-on differs depending on whether or not this delay time has elapsed.

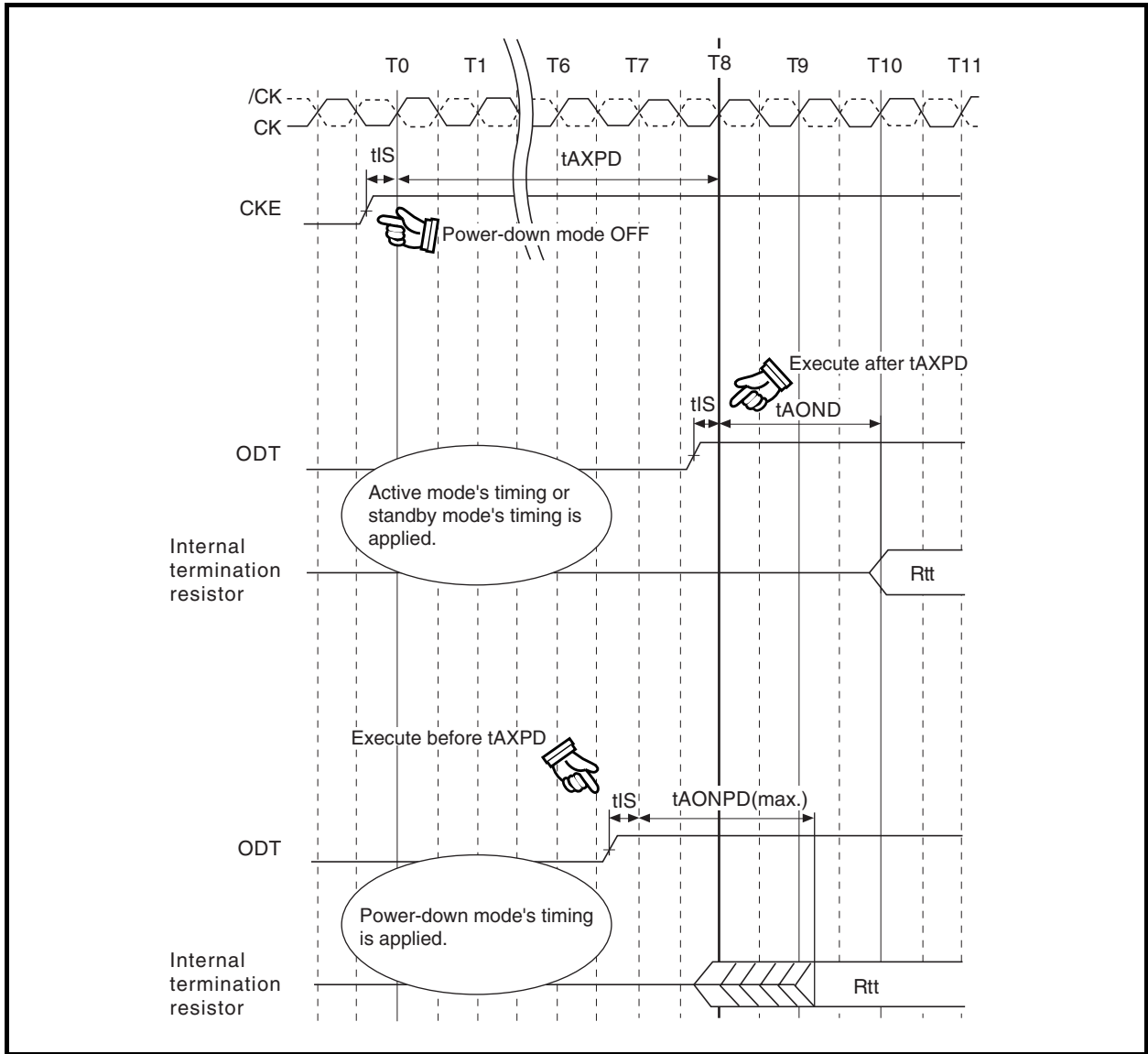


Figure 5-5 ODT ON Timing at Exiting Power-down Mode

5.6 ODT OFF timing at exiting power-down mode

Figure 5-6 shows the timing when ODT is set to OFF while exiting power-down mode.

The exit delay time (t_{AXPD}) must elapse before exiting power-down mode. The timing for ODT turn-off differs depending on whether or not this delay time has elapsed.

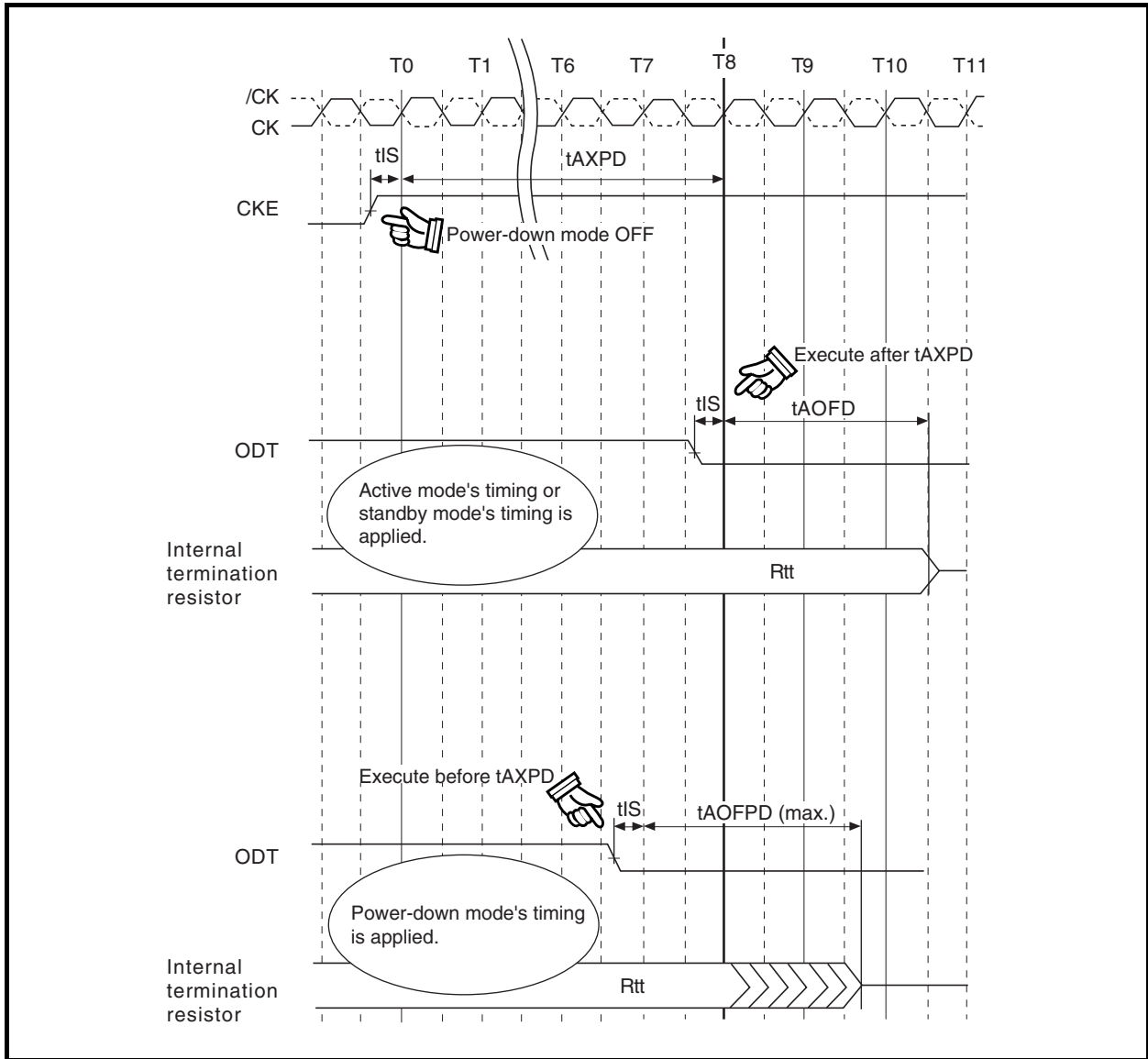


Figure 5-6 ODT OFF Timing at Exiting Power-down Mode

6. ODT in Self-refresh Mode

ODT is not supported during self-refresh mode.

The information in this document is current as April, 2007. The information is subject to change without notice.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

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