

New Function of DDR2 SDRAM Off-Chip Driver (OCD)

CAUTION

This document describes Off-Chip Driver (OCD), a new function that has been added to DDR2 SDRAM.

OCD function is no longer necessary for DDR2 SDRAM and often used in default setting.

For details about the functions, refer to the corresponding data sheet or user's manual.

In addition, operation and the numerical value that appear in this manual show the example of reference.

1. Overview of OCD

1.1 Drive performance and transition time

When the drive performance varies, the transition time (rise time or fall time) needed for an output signal to reach any specified voltage also varies.

Figure 1-1 shows an image of how the transition times of output signals differ depending on the drive performance.

Generally, a higher drive performance means a faster signal transition time (rise time or fall time). Conversely, a lower drive performance means a slower signal transition time (rise time or fall time).

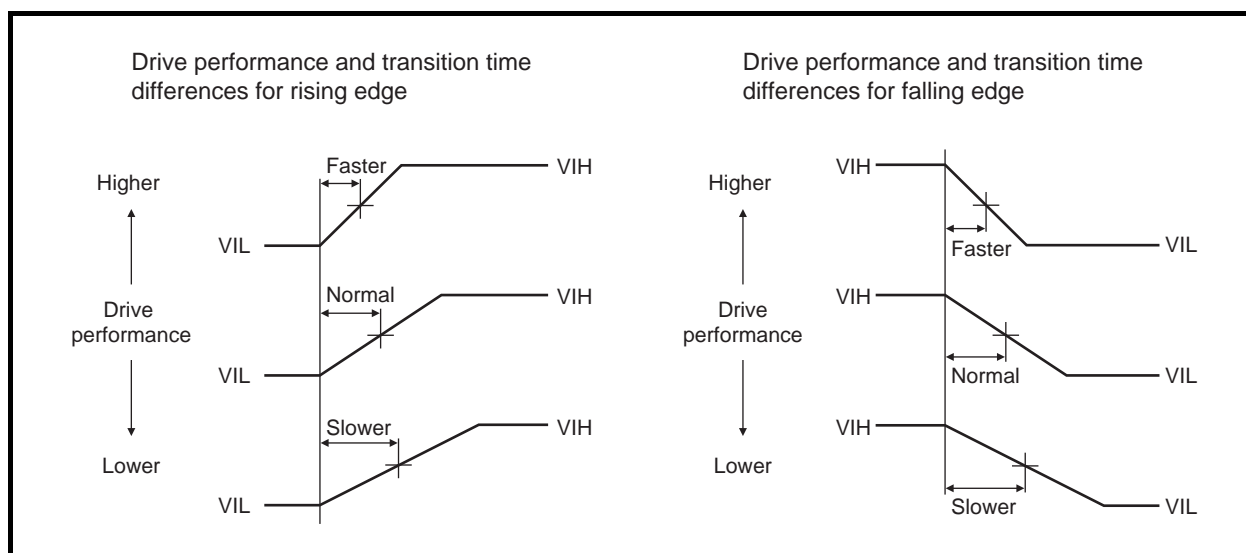


Figure 1-1 Drive Performance and Signal Transition Time

1.2 DQS signal, /DQS signal, and drive performance

The DQS and /DQS signals that are used by DDR2 SDRAM are phase related.

When the DQS and /DQS signals have the same drive performance, each signal's intermediate level and cross point also match.

However, if either signal has weaker (or stronger) drive performance than the other, the cross point and intermediate level do not match.

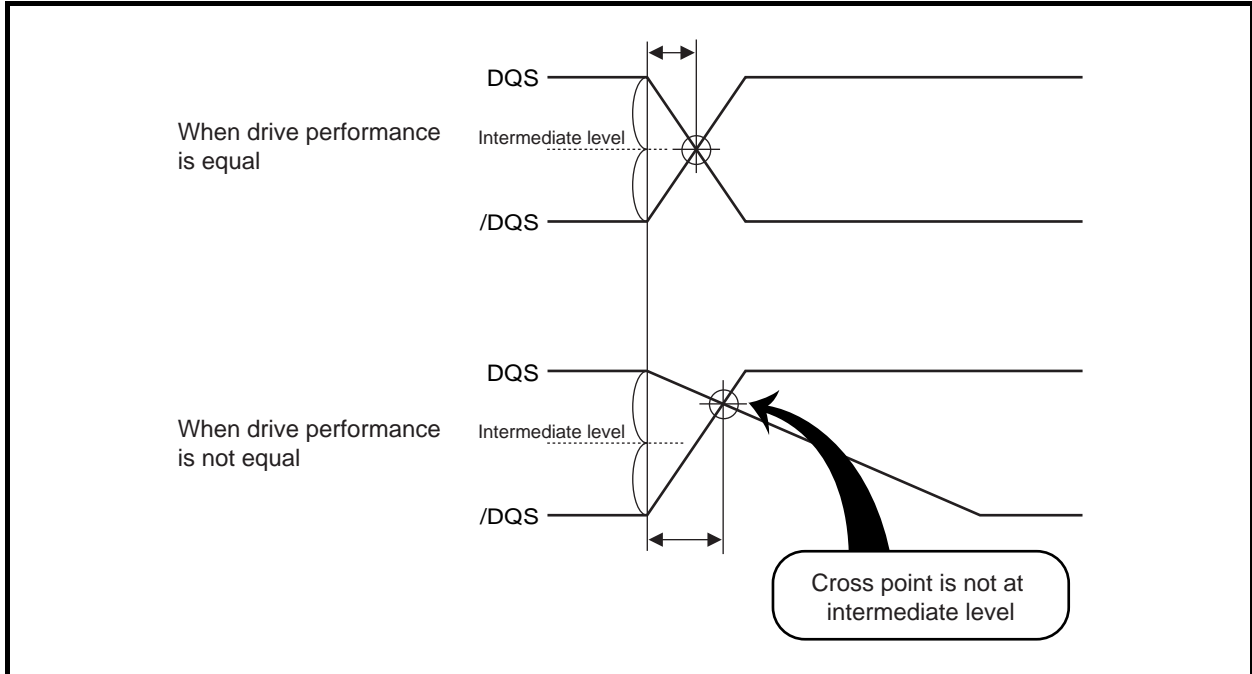


Figure 1-2 DQS Signal, /DQS Signal, and Drive performance

1.3 DQS signal, /DQS signal, and valid data window

DDR2 SDRAM uses the cross point between the DQS and /DQS signals as a reference clock for I/O data. The memory controller latches data from the DQ signal in synchronization with this reference clock. The DQ signal is referenced to distinguish the high and low levels of the VREF signal.

When the DQS and /DQS signals have different drive performances, the cross point between the DQS and /DQS signals will be offset from each signal's intermediate level. Consequently, a delay time (DQ-DQS skew) occurs between the cross point of the DQS and /DQS signals on the one hand and the cross point of the DQ and VREF signals on the other hand.

When such DQ-DQS skew exists, the time (valid data window) provided for latching data during data input or output is reduced. Reduction of this valid data window is a serious issue for DDR2 SDRAM, which require high-speed operations.

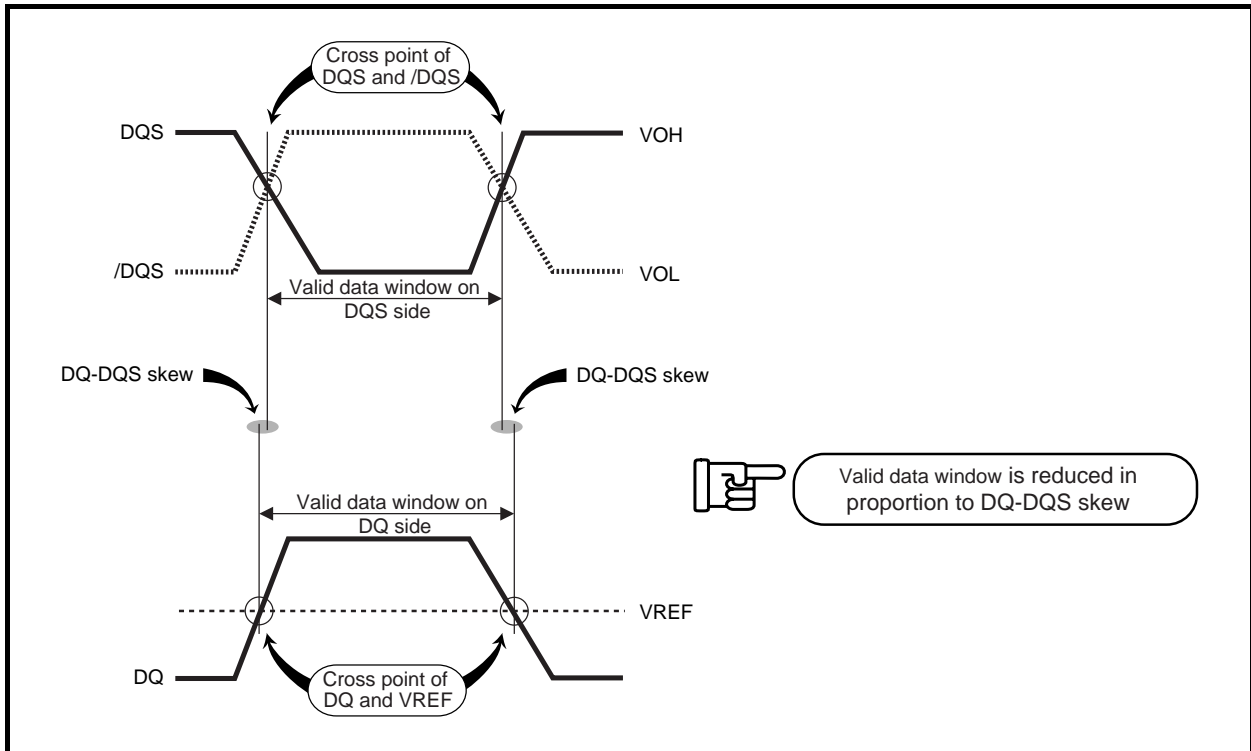


Figure 1-3 DQS Signal, /DQS Signal, and Valid Data Window

1.4 Extension of valid data window by voltage adjustment

OCD is used to adjust the impedance value of the DRAM's internal output driver. This function can adjust the voltage to equalize the pull-up resistance and pull-down resistance of the output signals (DQ, DQS, and /DQS).

When OCD is used to adjust the voltage, the cross point between the DQS and /DQS signals can be made to match the each signal's intermediate level. Optimizing the cross point between the DQS and /DQS signals minimizes the delay time for the cross point between the DQ and VREF signals.

When OCD is used to adjust the voltage with DDR2 SDRAM, DQ-DQS skew can be minimized, which maximizes the time (valid data window) provided for latching data when data is being input or output.

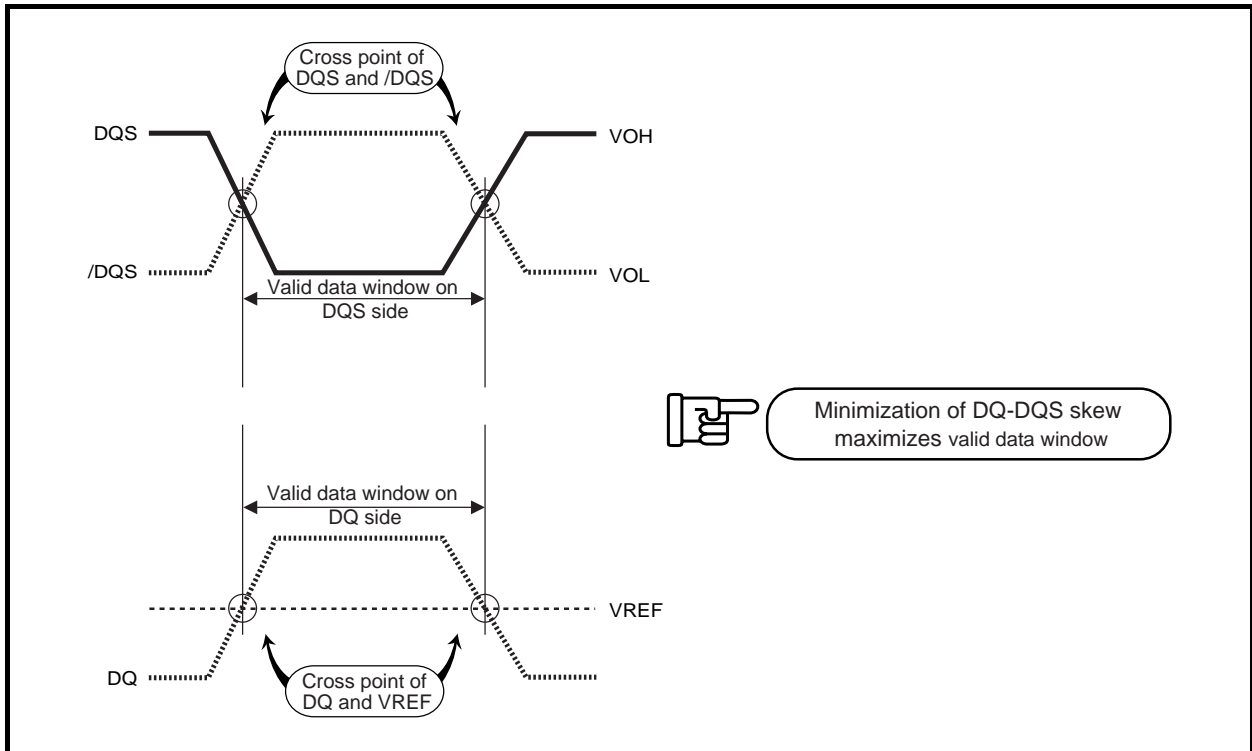


Figure 1-4 Expansion of Valid Data Window by Voltage Adjustment

2. Setting of OCD Impedance Value

The OCD impedance value is set by optimizing the impedance value of signals output by the DRAM while in drive mode, based on measurements made by the memory controller or an external measuring instrument.

During drive mode, an external device is used for comparison to determine the differential between the current impedance value and the target value (for SSTL_18, the target value is $18\pm 3\Omega$). When such a differential exists, the impedance is adjusted in adjustment mode. These comparison and adjustment steps are repeated until the optimum impedance value is set. When an OCD impedance value adjustment is being performed, all output pins are set to have the same impedance value.

NOTE

Impedance value measurement and comparison functions are not supported by DDR2 SDRAM.

Consequently, a memory controller or other external device must be used for these measurement and comparison operations.

2.1 OCD impedance adjustment method

Five operations are performed to adjust the OCD impedance: set drive (1) mode, set drive (0) mode, set adjustment mode, OCD calibration mode exit, and set OCD calibration default. All of these operations are selected via settings in EMRS (1) (Extended Mode Registers Set (1)).

To adjust the impedance value, the pull-up resistance and pull-down resistance must be adjusted separately. This is why drive (1) mode and drive (0) mode are set.

To switch to a different mode, OCD calibration must be canceled along with the current mode.

2.2 OCD impedance adjustment steps

To adjust the impedance value, the pull-up resistance and pull-down resistance must be adjusted separately. Consequently, drive (1) mode and drive (0) mode are set. It does not matter which drive mode is set first.

Once a drive mode is set, it is determined whether or not the current impedance value is the optimum value. If the impedance value needs to be adjusted, adjustment mode is set and the impedance value is adjusted. This is repeated until the impedance value becomes the optimum value.

To switch to a different mode or to exit, OCD calibration must be canceled along with the current mode.

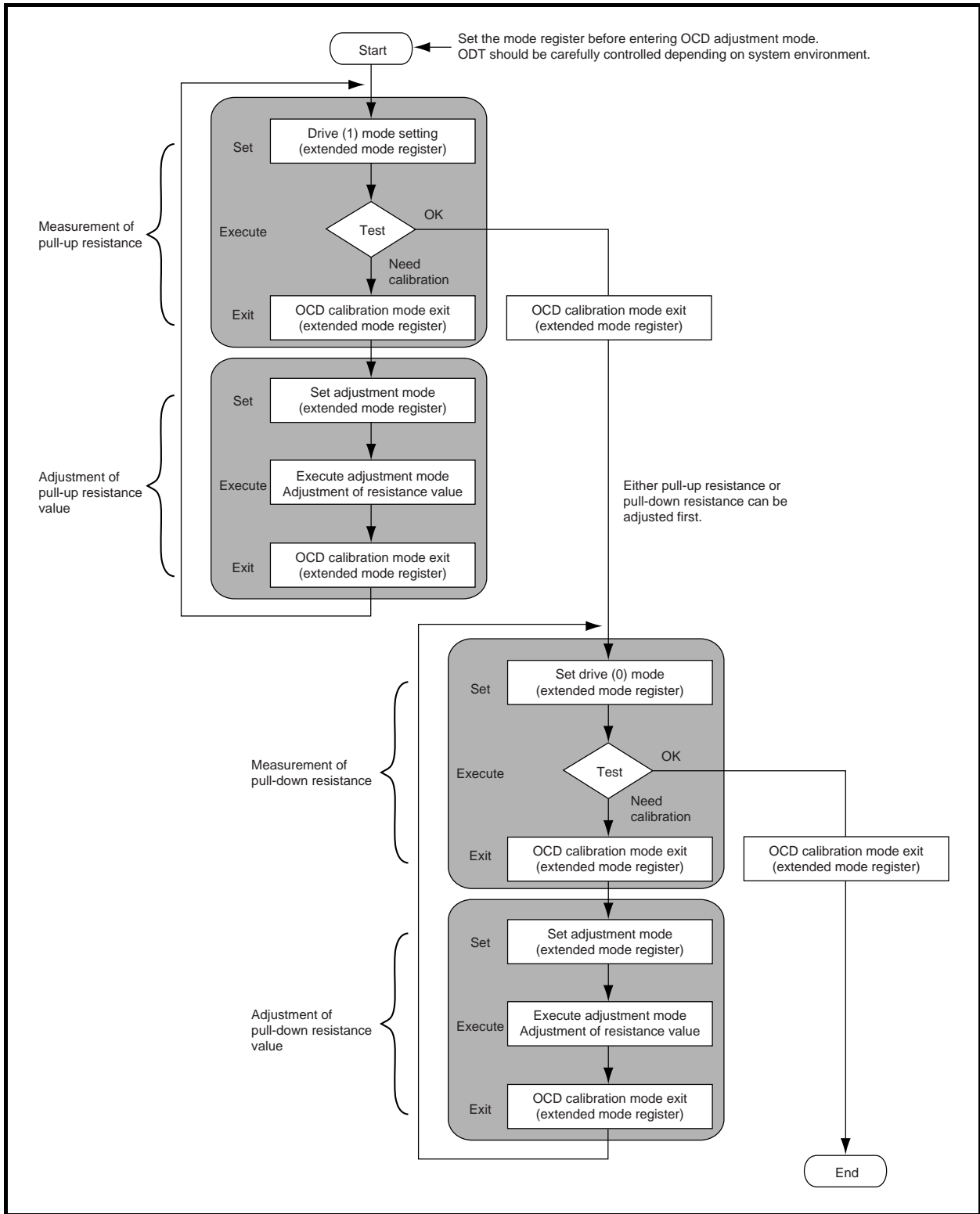


Figure 2-1 OCD Impedance Adjustment Flowchart

3. Setting of OCD Value

The OCD function's various modes are set via EMRS (1) (Extended Mode Registers Set (1)). Three bits (A7, A8, and A9) can be used to set any of five modes for OCD calibration: drive (1) mode, drive (0) mode, adjustment mode, OCD calibration mode exit, and OCD calibration default.

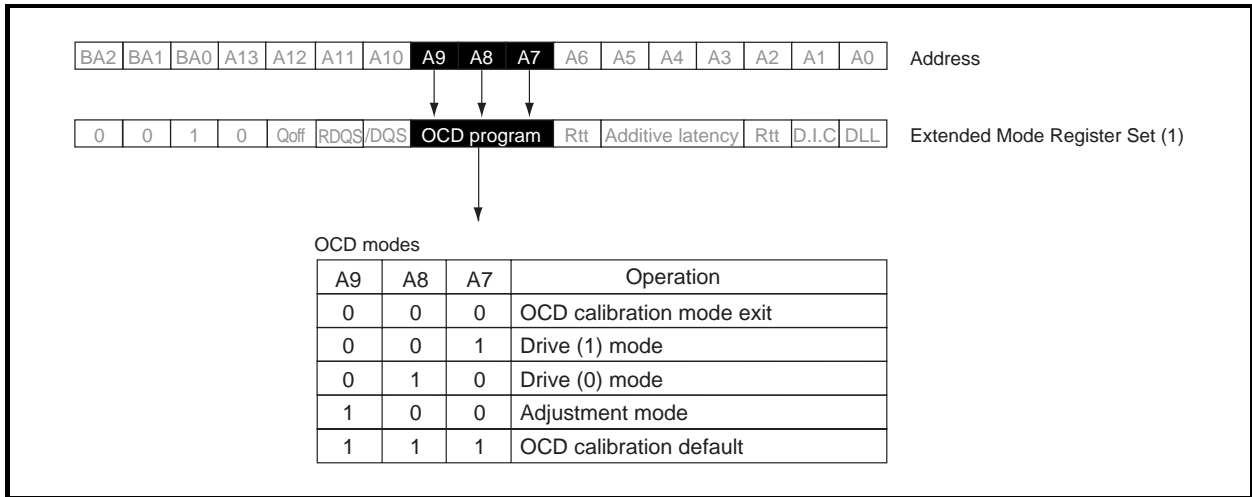


Figure 3-1 OCD Mode Settings via Extended Mode Register Set (1)

3.1 Drive (1) mode

When drive (1) mode is used, the existing status is set for the output level of output signals (DQ, DQS, and /DQS). An external device such as a memory controller must be used to measure the voltage level of the output signals (DQ, DQS, and /DQS) and determine whether or not the pull-up resistance is at the target value.

Once drive (1) mode has been set, the tOIT time must elapse before the output signals (DQ, DQS, and /DQS) are set to the output statuses listed in Table 2-1.

Table 3-1 Output Signals When Drive (1) Mode Is Set

Output Signal	Output Status
DQ	High level
DQS	High level
/DQS	Low level

These output statuses are maintained until the "OCD calibration mode exit" command is entered.

An external device is used to determine whether or not the optimum impedance value has been set for the output driver that drives the output signals (DQ, DQS, and /DQS). If this impedance value is not the optimum value, it must be reset in adjustment mode.

This cycle of measurement and adjustment is repeated until the optimum impedance value is set.

NOTE

Impedance value measurement and comparison functions are not supported by DDR2 SDRAM.

Consequently, a memory controller or other external device must be used for these measurement and comparison operations.

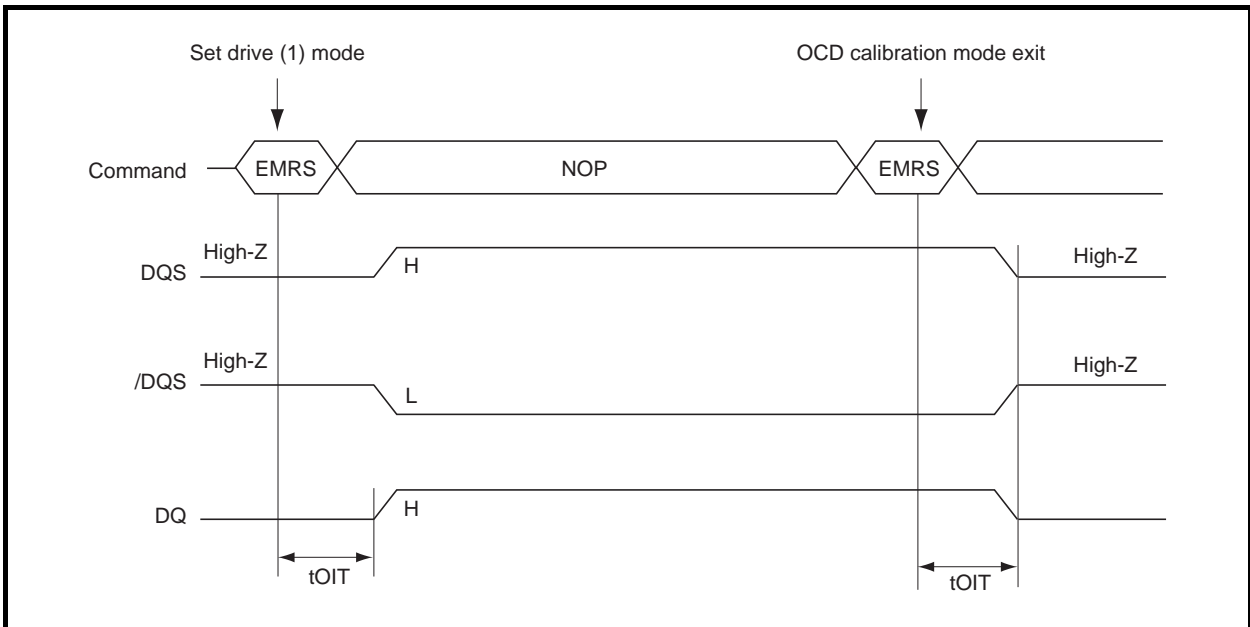


Figure 3-2 Drive (1) Mode Timing

3.2 Drive (0) mode

When drive (0) mode is used, the existing status is set for the output level of output signals (DQ, DQS, and /DQS). An external device such as a memory controller must be used to measure the voltage level of the output signals (DQ, DQS, and /DQS) and determine whether or not the pull-down resistance is at the target value.

Once drive (0) mode has been set, the tOIT time must elapse before the output signals (DQ, DQS, and /DQS) are set to the output statuses listed in Table 2-2.

Table 3-2 Output Signals When Drive (0) Mode Is Set

Output Signal	Output Status
DQ	Low level
DQS	Low level
/DQS	High level

These output statuses are maintained until the "OCD calibration mode exit" command is entered.

An external device is used to determine whether or not the optimum impedance value has been set for the output driver that drives the output signals (DQ, DQS, and /DQS). If this impedance value is not the optimum value, it must be reset in adjustment mode.

This cycle of measurement and adjustment is repeated until the optimum impedance value is set.

NOTE

Impedance value measurement and comparison functions are not supported by DDR2 SDRAM.

Consequently, a memory controller or other external device must be used for these measurement and comparison operations.

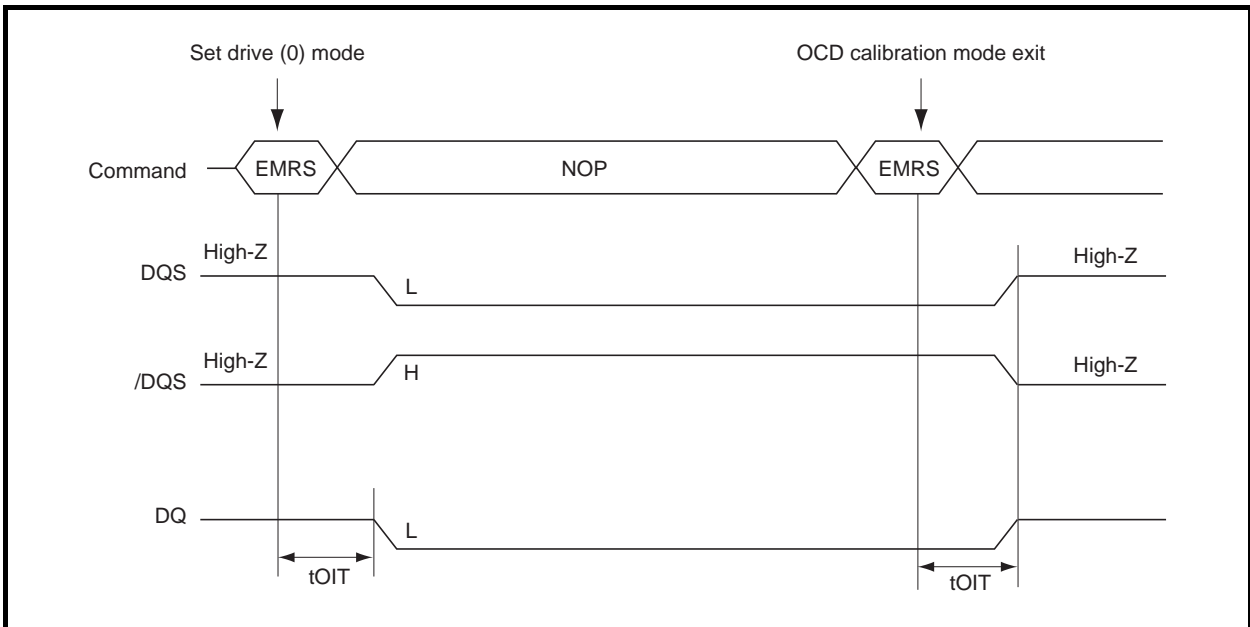


Figure 3-3 Drive (0) Mode Timing

3.3 Adjustment mode

Adjustment mode is used to adjust the output driver's impedance value. Since this impedance value can be adjusted among 16 levels, fine adjustment of the voltage can be performed to equalize the pull-up resistance and pull-down resistance of the output signals (DQ, DQS, and /DQS).

Once adjustment mode has been set, the write latency (WL) period must elapse, then the output driver's impedance value can be adjusted by input of four bursts of data to the DQ pin. If the output driver's impedance value has reached its limit, it cannot be adjusted upward or downward beyond that limit.

Before entering adjustment mode, the burst length must be set to "4". At that time, the input data must be input to all of the DQ pins at the same time.

Even after adjustment mode has been set, if posted CAS was used to enter commands before switching to adjustment mode, the commands are executed after the additive latency period has elapsed.

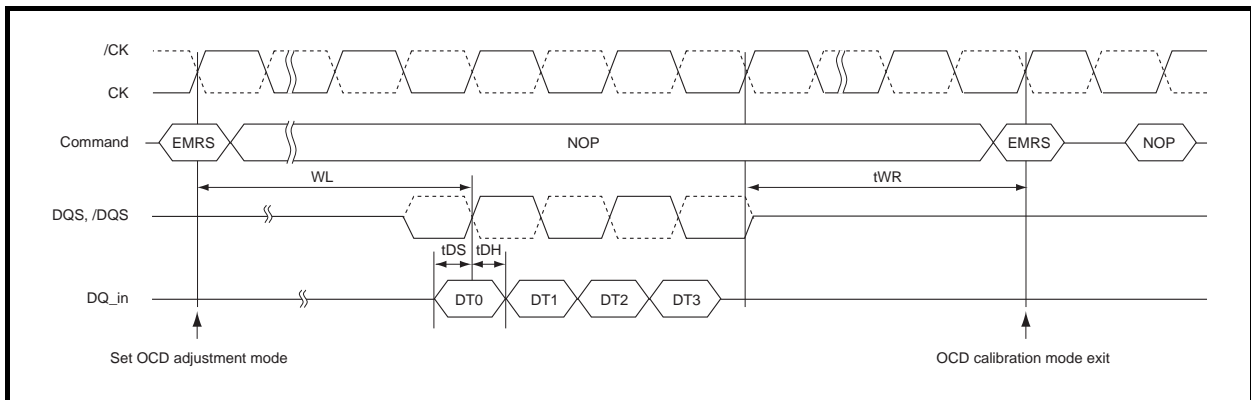


Figure 3-4 Adjustment Mode Timing

Table 3-3 Burst Data and Operations

Burst Data				Operation	
DT0	DT1	DT2	DT3	Pull-up Driver strength	Pull-down Driver strength
0	0	0	0	—	—
0	0	0	1	Increased by 1 step	—
0	0	1	0	Reduced by 1 step	—
0	1	0	0	—	Increased by 1 step
1	0	0	0	—	Reduced by 1 step
0	1	0	1	Increased by 1 step	Increased by 1 step
0	1	1	0	Reduced by 1 step	Increased by 1 step
1	0	0	1	Increased by 1 step	Reduced by 1 step
1	0	1	0	Reduced by 1 step	Reduced by 1 step
Other than above				Reserved	

REMARKS

1. "—" indicates no change (NOP).
2. If data other than shown above is entered, the status is the same as "—".

3.4 OCD calibration mode exit

When adjusting the OCD impedance value, the current mode must be exited before switching to another mode. The OCD calibration mode exit command is used to exit the current mode.

3.5 OCD calibration default

OCD calibration default mode sets the output driver's current impedance value to the default value. For further information, see the particular product's data sheet.

3.6 Example of impedance value test circuit

The comparison circuit shown in Figure 3-5 can be used to measure impedance values. This circuit is used by an external device to determine whether or not the impedance value of the output signals (DQ, DQS, and /DQS) is at the optimum value.

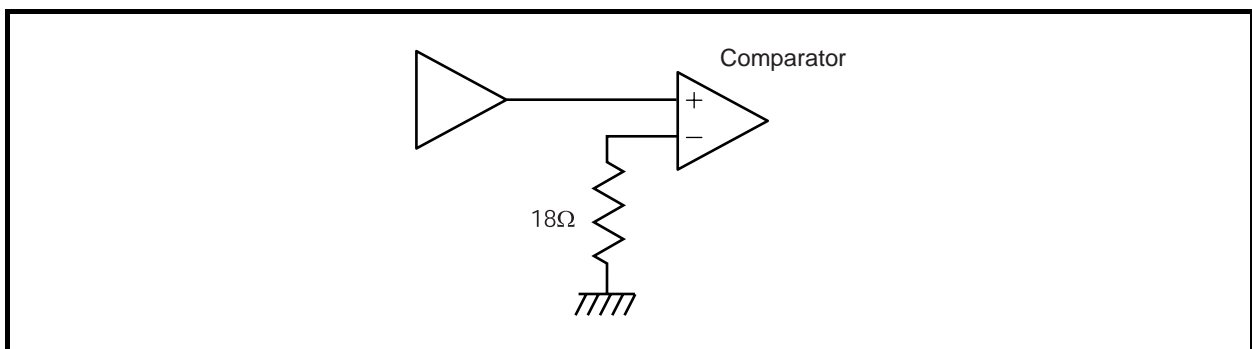


Figure 3-5 Impedance Value Test Circuit Example

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NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

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