TECHNICAL NOTE

DDR2 SDRAM TECHNOLOGY

CAUTION

This document describes new functions that have been added to DDR2 SDRAM.

For details about the functions, refer to the corresponding data sheet, user’s manual, or technical note.

In addition, operation and the numerical value that appear in this manual show the example of reference.

1. 4-bit Prefetch

DDR2 SDRAM achieves high-speed operation by 4-bit prefetch architecture.

In 4-bit prefetch architecture, DDR2 SDRAM can read/write 4 times the amount of data as an external bus from/to the memory cell array for every clock, and can be operated 4 times faster than the internal bus operation frequency.

- External clock frequency = 2 times faster than internal bus operation frequency
- Double data rate output = 2 times faster than external clock frequency

A comparison between DDR2 SDRAM, DDR SDRAM, and SDR SDRAM with a DRAM core operating frequency of 133MHz is shown below.

Table 1-1 Comparison between DDR2 SDRAM, DDR SDRAM, and SDR SDRAM

Item	**DDR2 SDRAM**	**DDR SDRAM**	**SDR SDRAM**
Prefetch	4-bit	2-bit	1-bit
Internal bus operating frequency	133MHz	133MHz	133MHz
External clock frequency	266MHz	133MHz	133MHz
Data bus speed	533Mbps	266Mbps	133Mbps

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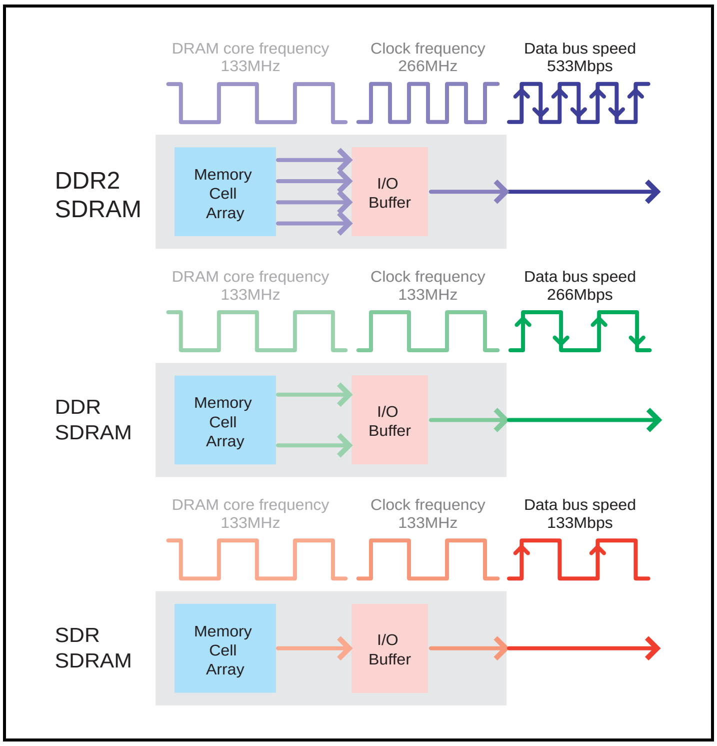

Figure 1-1 Comparison between DDR2 SDRAM, DDR SDRAM, and SDR SDRAM

2. ODT (On Die Termination)

In DDR2 SDRAM, the mount termination register conventionally mounted on the motherboard is incorporated inside the DRAM chip.

The DRAM controller can set the termination register for each signal (data I/O, differential data strobe, and write data mask) on and off.

- Improved signal integrity by controlling reflected noise on the transfer line.
- Reduction of parts costs by reducing the parts counts on the motherboard.
- Easier system design by eliminating the complicated placement and routing for the termination register.

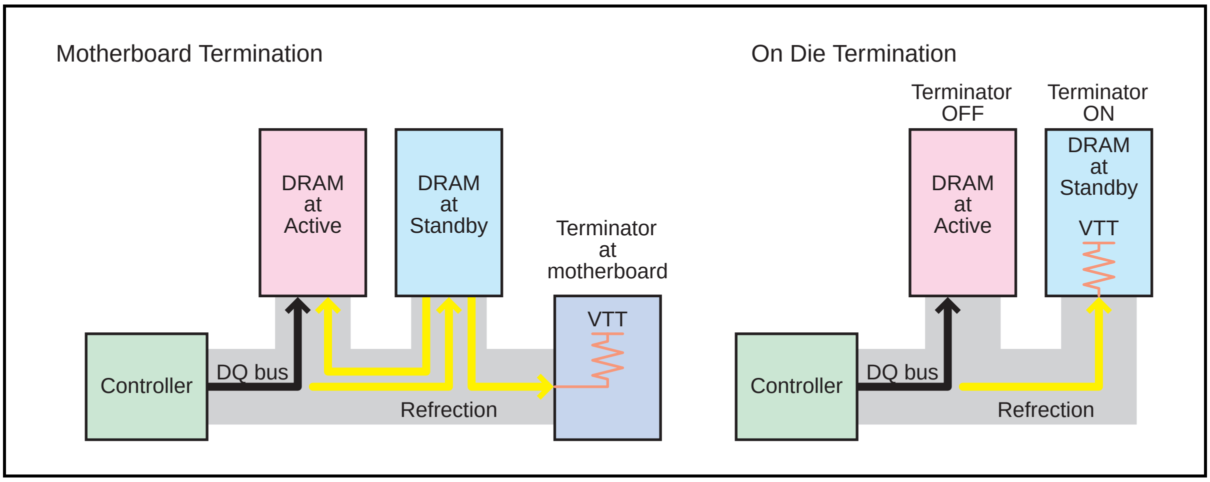

Figure 2-1 Comparison between Motherboard Termination and On Die Termination

3. OCD (Off-Chip Driver) Calibration

DDR2 SDRAM improves signal integrity by OCD calibration. In OCD calibration, the I/O driver resistance is set to adjust the voltage to equalize the pull-up/pull-down resistance.

- Improved signal integrity by minimizing DQ-DQS skew.
- Improved signal quality by controlling the overshoot and undershoot.
- Absorbing process variations from each DRAM supplier by I/O driver voltage calibration.

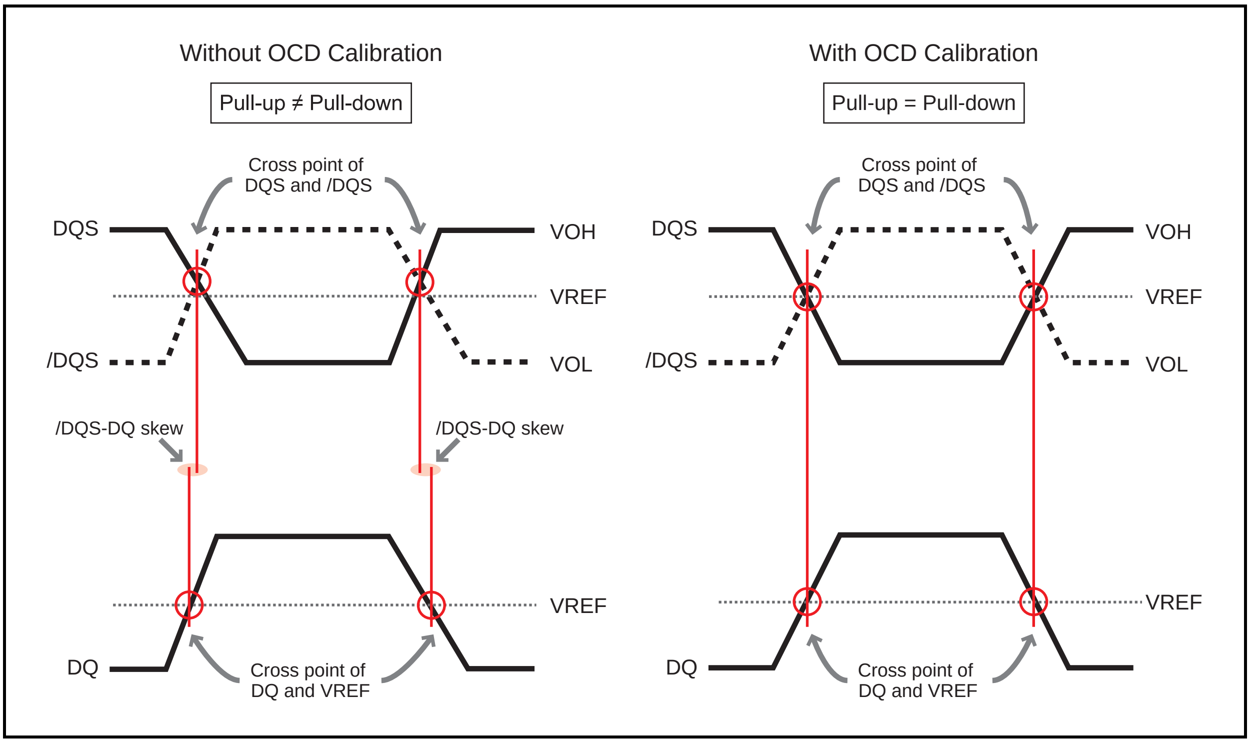

Figure 3-1 Comparison between "Without OCD Calibration" and "With OCD Calibration"

4. Posted CAS & Additive Latency (AL)

In a posted CAS operation, a CAS signal (read/write command) can be input to the next clock after RAS signal (active command) input. The CAS command is held by the DRAM side and executed after the additive latency (0, 1, 2, 3, and 4)

- Easier controller design by avoiding collision on the command bus.
- Improved command and data bus efficiency due to simple command order.
- Improved practical memory bandwidth without bubble.

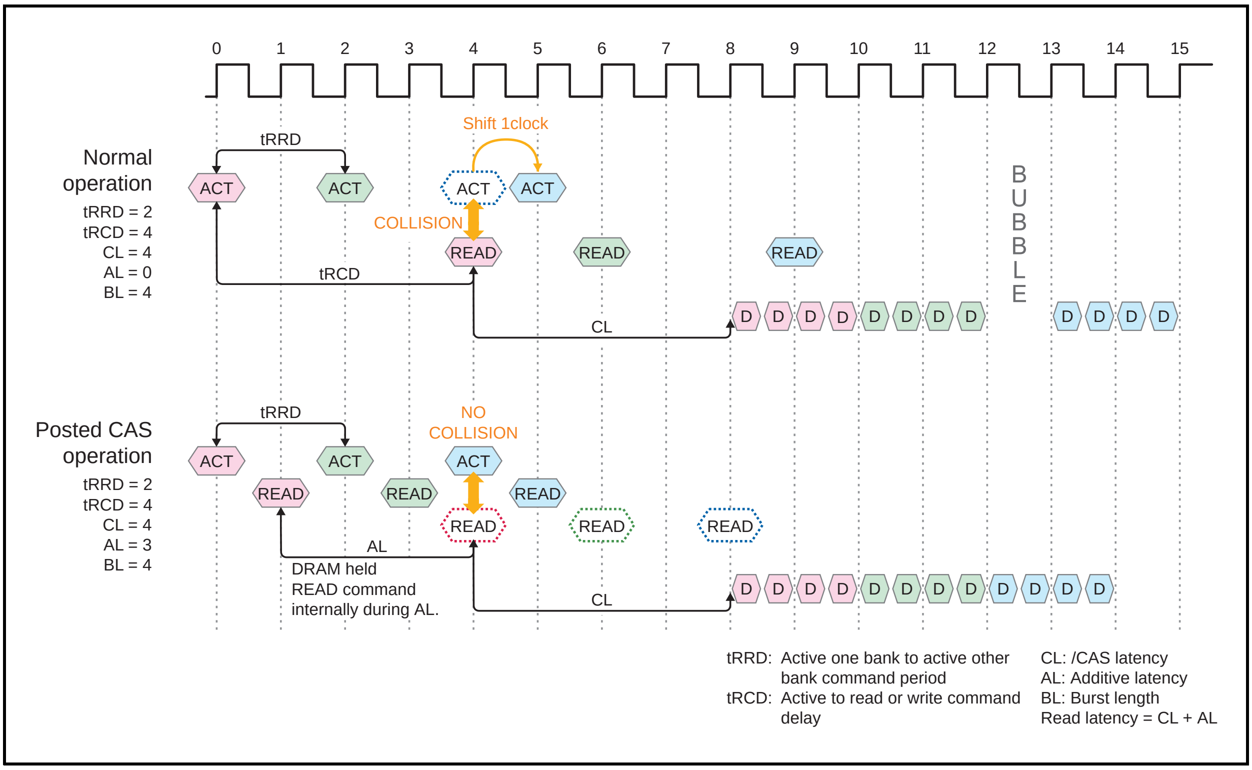

Figure 4-1 Comparison between Normal Operation and Posted CAS Operation

The information in this document is current as August, 2005. The information is subject to change without notice.

NOTES FOR CMOS DEVICES

① **PRECAUTION AGAINST ESD FOR MOS DEVICES**

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

② **HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES**

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

③ **STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

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