

**2G bits DDR2 SDRAM****EDE2104AASE (512M words × 4 bits)  
EDE2108AASE (256M words × 8 bits)****Description**

The EDE2104AASE is a 2G bits DDR2 SDRAM organized as 67,108,864 words × 4 bits × 8 banks.

The EDE2108AASE is a 2G bits DDR2 SDRAM organized as 33,554,432 words × 8 bits × 8 banks.

They are packaged in 68-ball FBGA package.

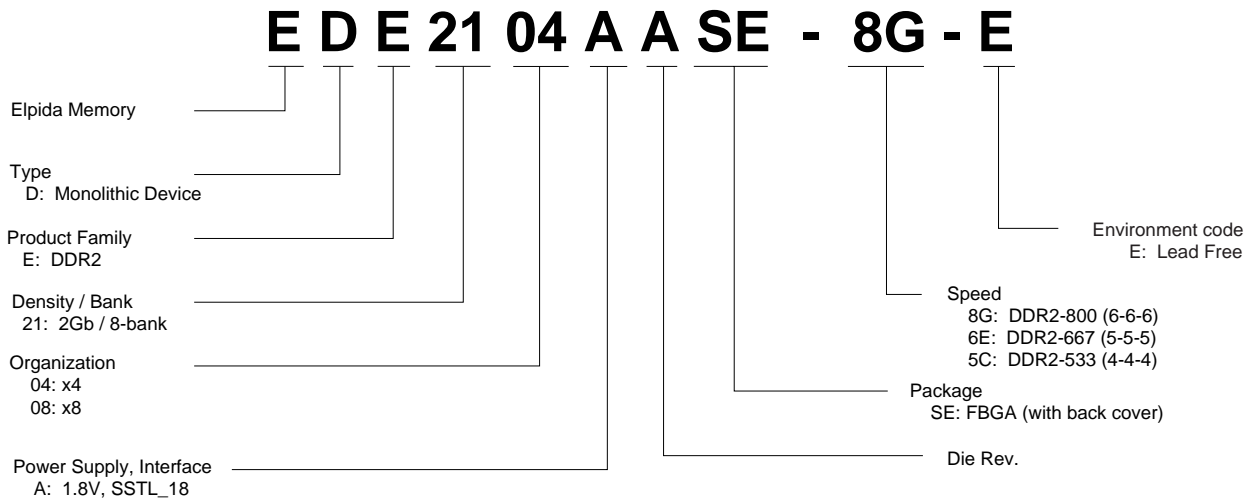
**Features**

- Power supply: VDD, VDDQ = 1.8V ± 0.1V
- Double-data-rate architecture: two data transfers per clock cycle
- Bi-directional, differential data strobe (DQS and /DQS) is transmitted/received with data, to be used in capturing data at the receiver
- DQS is edge aligned with data for READs: center-aligned with data for WRITEs
- Differential clock inputs (CK and /CK)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge: data and data mask referenced to both edges of DQS
- 8 internal banks for concurrent operation
- Data mask (DM) for write data
- Burst lengths: 4, 8
- /CAS Latency (CL): 3, 4, 5, 6
- Auto precharge operation for each burst access
- Auto refresh and self refresh modes
- Average refresh period
  - 7.8μs at 0°C ≤ TC ≤ +85°C
  - 3.9μs at +85°C < TC ≤ +95°C
- SSTL\_18 compatible I/O
- Posted CAS by programmable additive latency for better command and data bus efficiency
- Off-Chip-Driver Impedance Adjustment and On-Die-Termination for better signal quality
- Programmable RDQS, /RDQS output for making × 8 organization compatible to × 4 organization
- /DQS, (/RDQS) can be disabled for single-ended Data Strobe operation.
- Programmable Partial Array Self Refresh
- FBGA package with lead free solder (Sn-Ag-Cu)
  - RoHs compliant

## Ordering Information

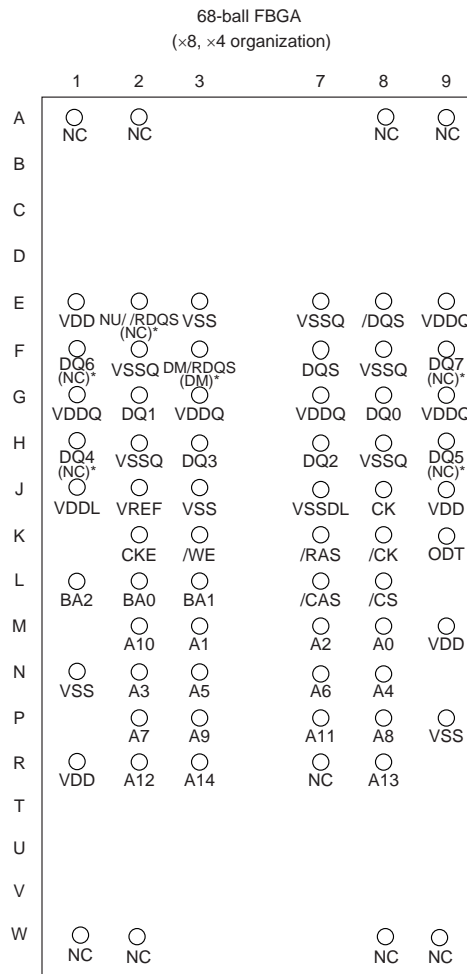
Part number	Mask version	Organization (words × bits)	Internal Banks	Speed bin (CL-tRCD-tRP)	Package
EDE2104AASE-8G-E	A	512M × 4	8	DDR2-800 (6-6-6)	68-ball FBGA
EDE2104AASE-6E-E				DDR2-667 (5-5-5)	
EDE2104AASE-5C-E				DDR2-533 (4-4-4)	
EDE2108AASE-8G-E		256M × 8		DDR2-800 (6-6-6)	
EDE2108AASE-6E-E				DDR2-667 (5-5-5)	
EDE2108AASE-5C-E				DDR2-533 (4-4-4)	

## Part Number



## Pin Configurations

/xxx indicates active low signal.



(Top view)

Note: ( ) \* marked pins are for ×4 organization.

Pin name	Function	Pin name	Function
A0 to A14	Address inputs	ODT	ODT control
BA0, BA1, BA2	Bank select	VDD	Supply voltage for internal circuit
DQ0 to DQ7	Data input/output	VSS	Ground for internal circuit
DQS, /DQS	Differential data strobe	VDDQ	Supply voltage for DQ circuit
RDQS, /RDQS	Differential data strobe for read	VSSQ	Ground for DQ circuit
/CS	Chip select	VREF	Input reference voltage
/RAS, /CAS, /WE	Command input	VDDL	Supply voltage for DLL circuit
CKE	Clock enable	VSSDL	Ground for DLL circuit
CK, /CK	Differential clock input	NC* <sup>1</sup>	No connection
DM	Write data mask	NU* <sup>2</sup>	Not usable

Notes: 1. Not internally connected with die.

2. Don't use other than reserved functions.

**NOTES FOR CMOS DEVICES****① PRECAUTION AGAINST ESD FOR MOS DEVICES**

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

**② HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES**

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

**③ STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

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**[Product usage]**

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**[Usage environment]**

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