

**512MB DDR3 SDRAM SO-DIMM****EBJ51UE6BASA (64M words × 64 bits, 1 Rank)****Specifications**

- Density: 512MB
- Organization
  - 64M words × 64 bits, 1 rank
- Mounting 4 pieces of 1G bits DDR3 SDRAM sealed in FBGA
- Package: 204-pin socket type small outline dual in line memory module (SO-DIMM)
  - PCB height: 30.0mm
  - Lead pitch: 0.6mm
  - Lead-free (RoHS compliant)
- Power supply: VDD = 1.5V ± 0.075V
- Data rate: 1333Mbps/1066Mbps/800Mbps (max.)
- Eight internal banks for concurrent operation (components)
- Interface: SSTL\_15
- Burst lengths (BL): 8 and 4 with Burst Chop (BC)
- /CAS Latency (CL): 5, 6, 7, 8, 9
- /CAS write latency (CWL): 5, 6, 7
- Precharge: auto precharge option for each burst access
- Refresh: auto-refresh, self-refresh
- Refresh cycles
  - Average refresh period
    - 7.8μs at 0°C ≤ TC ≤ +85°C
    - 3.9μs at +85°C < TC ≤ +95°C
- Operating case temperature range
  - TC = 0°C to +95°C

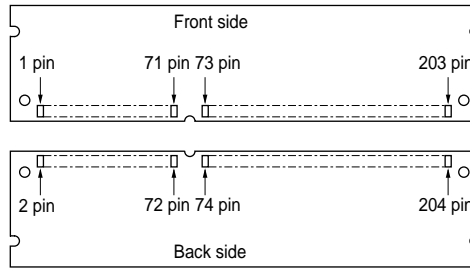
**Features**

- Double-data-rate architecture; two data transfers per clock cycle
- The high-speed data transfer is realized by the 8 bits prefetch pipelined architecture
- Bi-directional differential data strobe (DQS and /DQS) is transmitted/received with data for capturing data at the receiver
- DQS is edge-aligned with data for READs; center-aligned with data for WRITEs
- Differential clock inputs (CK and /CK)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Data mask (DM) for write data
- Posted /CAS by programmable additive latency for better command and data bus efficiency
- On-Die-Termination (ODT) for better signal quality
  - Synchronous ODT
  - Dynamic ODT
  - Asynchronous ODT
- Multi Purpose Register (MPR) for temperature read out
- ZQ calibration for DQ drive and ODT
- Programmable Partial Array Self-Refresh (PASR)
- /RESET pin for Power-up sequence and reset function
- SRT range:
  - Normal/extended
  - Auto/manual self-refresh
- Programmable Output driver impedance control

## Ordering Information

Part number	Data rate Mbps (max.)	Component JEDEC speed bin (CL-tRCD-tRP)	Package	Contact pad	Mounted devices
EBJ51UE6BASA-DG-E	1333	DDR3-1333G (8-8-8)	204-pin SO-DIMM (lead-free)	Gold	EDJ1116BASE-DG-E
EBJ51UE6BASA-DJ-E		DDR3-1333H (9-9-9)			EDJ1116BASE-DG-E EDJ1116BASE-DJ-E
EBJ51UE6BASA-AC-E	1066	DDR3-1066E (6-6-6)			EDJ1116BASE-AC-E
EBJ51UE6BASA-AE-E		DDR3-1066F (7-7-7)			EDJ1116BASE-DG-E EDJ1116BASE-DJ-E EDJ1116BASE-AC-E EDJ1116BASE-AE-E
EBJ51UE6BASA-AG-E		DDR3-1066G (8-8-8)			EDJ1116BASE-DG-E EDJ1116BASE-DJ-E EDJ1116BASE-AC-E EDJ1116BASE-AE-E EDJ1116BASE-AG-E
EBJ51UE6BASA-8A-E	800	DDR3-800D (5-5-5)			EDJ1116BASE-DG-E EDJ1116BASE-DJ-E EDJ1116BASE-AC-E EDJ1116BASE-AE-E EDJ1116BASE-AG-E EDJ1116BASE-8A-E
EBJ51UE6BASA-8C-E		DDR3-800E (6-6-6)			EDJ1116BASE-DG-E EDJ1116BASE-DJ-E EDJ1116BASE-AC-E EDJ1116BASE-AE-E EDJ1116BASE-AG-E EDJ1116BASE-8A-E EDJ1116BASE-8C-E

## Pin Configurations



Front side			Back side				
Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	VREFDQ	103	/CK0	2	VSS	104	/CK1
3	VSS	105	VDD	4	DQ4	106	VDD
5	DQ0	107	A10 (AP)	6	DQ5	108	BA1
7	DQ1	109	BA0	8	VSS	110	/RAS
9	VSS	111	VDD	10	/DQS0	112	VDD
11	DM0	113	/WE	12	DQS0	114	/CS0
13	VSS	115	/CAS	14	VSS	116	ODT0
15	DQ2	117	VDD	16	DQ6	118	VDD
17	DQ3	119	NC	18	DQ7	120	NC
19	VSS	121	NC	20	VSS	122	NC
21	DQ8	123	VDD	22	DQ12	124	VDD
23	DQ9	125	NC	24	DQ13	126	VREFCA
25	VSS	127	VSS	26	VSS	128	VSS
27	/DQS1	129	DQ32	28	DM1	130	DQ36
29	DQS1	131	DQ33	30	/RESET	132	DQ37
31	VSS	133	VSS	32	VSS	134	VSS
33	DQ10	135	/DQS4	34	DQ14	136	DM4
35	DQ11	137	DQS4	36	DQ15	138	VSS
37	VSS	139	VSS	38	VSS	140	DQ38
39	DQ16	141	DQ34	40	DQ20	142	DQ39
41	DQ17	143	DQ35	42	DQ21	144	VSS
43	VSS	145	VSS	44	VSS	146	DQ44
45	/DQS2	147	DQ40	46	DM2	148	DQ45
47	DQS2	149	DQ41	48	VSS	150	VSS
49	VSS	151	VSS	50	DQ22	152	/DQS5
51	DQ18	153	DM5	52	DQ23	154	DQS5
53	DQ19	155	VSS	54	VSS	156	VSS
55	VSS	157	DQ42	56	DQ28	158	DQ46
57	DQ24	159	DQ43	58	DQ29	160	DQ47
59	DQ25	161	VSS	60	VSS	162	VSS
61	VSS	163	DQ48	62	/DQS3	164	DQ52
63	DM3	165	DQ49	64	DQS3	166	DQ53
65	VSS	167	VSS	66	VSS	168	VSS
67	DQ26	169	/DQS6	68	DQ30	170	DM6

Front side				Back side			
Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
69	DQ27	171	DQS6	70	DQ31	172	VSS
71	VSS	173	VSS	72	VSS	174	DQ54
73	CKE0	175	DQ50	74	NC	176	DQ55
75	VDD	177	DQ51	76	VDD	178	VSS
77	NC	179	VSS	78	NC	180	DQ60
79	BA2	181	DQ56	80	NC	182	DQ61
81	VDD	183	DQ57	82	VDD	184	VSS
83	A12 (/BC)	185	VSS	84	A11	186	/DQS7
85	A9	187	DM7	86	A7	188	DQS7
87	VDD	189	VSS	88	VDD	190	VSS
89	A8	191	DQ58	90	A6	192	DQ62
91	A5	193	DQ59	92	A4	194	DQ63
93	VDD	195	VSS	94	VDD	196	VSS
95	A3	197	SA0	96	A2	198	/EVENT
97	A1	199	VDDSPD	98	A0	200	SDA
99	VDD	201	SA1	100	VDD	202	SCL
101	CK0	203	VTT	102	CK1	204	VTT

**Pin Description**

Pin name	Function
	Address input
A0 to A12	Row address      A0 to A12 Column address    A0 to A9
A10 (AP)	Auto precharge
A12 (/BC)	Burst chop
BA0, BA1, BA2	Bank select address
DQ0 to DQ63	Data input/output
/RAS	Row address strobe command
/CAS	Column address strobe command
/WE	Write enable
/CS0	Chip select
CKE0	Clock enable
CK0, CK1	Clock input
/CK0, /CK1	Differential clock input
DQS0 to DQS7, /DQS0 to /DQS7	Input and output data strobe
DM0 to DM7	Input mask
SCL	Clock input for serial PD
SDA	Data input/output for serial PD
SA0, SA1	Serial address input
VDD	Power for internal circuit
VDDSPD	Power for serial EEPROM
VREFCA	Reference voltage for CA
VREFDQ	Reference voltage for DQ
VSS	Ground
VTT	I/O termination supply for SDRAM
/RESET	Set DRAM to known state
ODT0	ODT control
/EVENT	Temperature event pin
NC	No connection

Serial PD Matrix

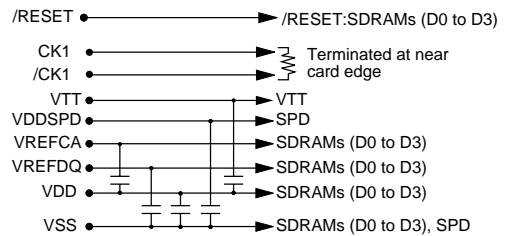
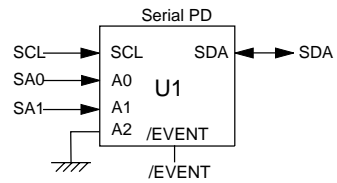
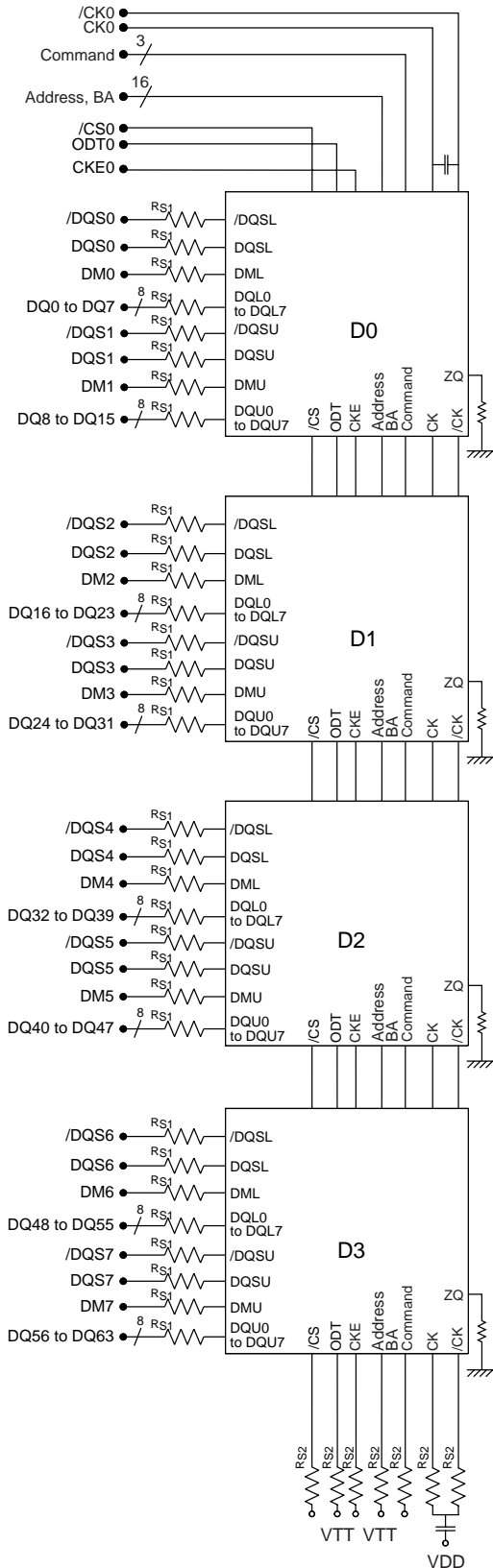
Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
0	Number of serial PD bytes written/SPD device size/CRC coverage	1	0	0	1	0	0	1	0	92H	CRC 0-116/256/176
1	SPD revision	0	0	0	0	0	1	0	1	05H	Revision 0.5
2	Key byte/DRAM device type	0	0	0	0	1	0	1	1	0BH	DDR3 SDRAM
3	Key byte/module type	0	0	0	0	0	0	1	1	03H	SO-DIMM
4	SDRAM density and banks	0	0	0	0	0	0	1	0	02H	1G bits, 8 banks
5	SDRAM addressing	0	0	0	0	1	0	0	1	09H	13 rows, 10 columns
6	Reserved	0	0	0	0	0	0	0	0	00H	—
7	Module organization	0	0	0	0	0	0	1	0	02H	1 rank/×16 bits
8	Module memory bus width	0	0	0	0	0	0	1	1	03H	64 bits / non-ECC
9	Fine timebase (FTB) dividend/divisor	0	1	0	1	0	0	1	0	52H	5 / 2
10	Medium timebase (MTB) dividend	0	0	0	0	0	0	0	1	01H	1
11	Medium timebase (MTB) divisor	0	0	0	0	1	0	0	0	08H	8
12	SDRAM minimum cycle time (tCK (min.)) -DG, -DJ	0	0	0	0	1	1	0	0	0CH	1.5ns
	-AC, -AE, -AG	0	0	0	0	1	1	1	1	0FH	1.875ns
	-8A, -8C	0	0	0	1	0	1	0	0	14H	2.5ns
13	Reserved	0	0	0	0	0	0	0	0	00H	—
14	SDRAM /CAS latencies supported, LSB -DG	0	0	1	1	1	1	1	0	3EH	CL = 5, 6, 7, 8, 9
	-DJ	0	0	1	1	0	1	0	0	34H	CL = 6, 8, 9
	-AC	0	0	0	1	1	1	1	0	1EH	CL = 5, 6, 7, 8
	-AE	0	0	0	1	1	1	0	0	1CH	CL = 6, 7, 8
	-AG	0	0	0	1	0	1	0	0	14H	CL = 6, 8
	-8A	0	0	0	0	0	1	1	0	06H	CL = 5, 6
	-8C	0	0	0	0	0	1	0	0	04H	CL = 6
15	SDRAM /CAS latencies supported, MSB	0	0	0	0	0	0	0	0	00H	—
16	SDRAM minimum /CAS latencies time (tAA (min.)) -DG	0	1	1	0	0	0	0	0	60H	12ns
	-DJ	0	1	1	0	1	1	0	0	6CH	13.5ns
	-AC	0	1	0	1	1	0	1	0	5AH	11.25ns
	-AE	0	1	1	0	1	0	0	1	69H	13.125ns
	-AG	0	1	1	1	1	0	0	0	78H	15ns
	-8A	0	1	1	0	0	1	0	0	64H	12.5ns
	-8C	0	1	1	1	1	0	0	0	78H	15ns
17	SDRAM write recovery time (tWR)	0	1	1	1	1	0	0	0	78H	15ns

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
18	SDRAM minimum /RAS to /CAS delay (tRCD) -DG	0	1	1	0	0	0	0	0	60H	12ns
	-DJ	0	1	1	0	1	1	0	0	6CH	13.5ns
	-AC	0	1	0	1	1	0	1	0	5AH	11.25ns
	-AE	0	1	1	0	1	0	0	1	69H	13.125ns
	-AG	0	1	1	1	1	0	0	0	78H	15ns
	-8A	0	1	1	0	0	1	0	0	64H	12.5ns
	-8C	0	1	1	1	1	0	0	0	78H	15ns
19	SDRAM minimum row active to row active delay (tRRD) -DG, -DJ	0	0	1	1	1	1	0	0	3CH	7.5ns
	-AC, -AE, -AG, -8A, -8C	0	1	0	1	0	0	0	0	50H	10ns
20	SDRAM minimum row precharge time (tRP) -DG	0	1	1	0	0	0	0	0	60H	12ns
	-DJ	0	1	1	0	1	1	0	0	6CH	13.5ns
	-AC	0	1	0	1	1	0	1	0	5AH	11.25ns
	-AE	0	1	1	0	1	0	0	1	69H	13.125ns
	-AG	0	1	1	1	1	0	0	0	78H	15ns
	-8A	0	1	1	0	0	1	0	0	64H	12.5ns
	-8C	0	1	1	1	1	0	0	0	78H	15ns
21	SDRAM upper nibbles for tRAS and tRC	0	0	0	1	0	0	0	1	11H	
22	SDRAM minimum active to precharge time (tRAS), LSB -DG, -DJ	0	0	1	0	0	0	0	0	20H	36ns
	-AC, -AE, -AG, -8A, -8C	0	0	1	0	1	1	0	0	2CH	37.5ns
23	SDRAM minimum active to active /auto-refresh time (tRC), LSB -DG	1	0	0	0	0	0	0	0	80H	48ns
	-DJ	1	0	0	0	1	1	0	0	8CH	49.5ns
	-AC	1	0	0	0	0	1	1	0	86H	48.75ns
	-AE	1	0	0	1	0	1	0	1	95H	50.625ns
	-AG	1	0	1	0	0	1	0	0	A4H	52.5ns
	-8A	1	0	0	1	0	0	0	0	90H	50ns
	-8C	1	0	1	0	0	1	0	0	A4H	52.5ns
24	SDRAM minimum refresh recovery time delay (tRFC), LSB	0	1	1	1	0	0	0	0	70H	110ns
25	SDRAM minimum refresh recovery time delay (tRFC), MSB	0	0	0	0	0	0	1	1	03H	110ns
26	SDRAM minimum internal write to read command delay (tWTR)	0	0	1	1	1	1	0	0	3CH	7.5ns
27	SDRAM minimum internal read to precharge command delay (tRTP)	0	0	1	1	1	1	0	0	3CH	7.5ns
28	Upper nibble for tFAW	0	0	0	0	0	0	0	1	01H	
29	Minimum four activate window delay time (tFAW) -DG, -DJ	0	1	1	0	1	0	0	0	68H	45ns
	-AC, -AE, -AG, -8A, -8C	1	0	0	1	0	0	0	0	90H	50ns
30	SDRAM output drivers supported	1	0	0	0	0	0	1	1	83H	DLL-off / RZQ/6, 7

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
31	SDRAM refresh options	1	0	0	0	1	0	0	0	88CH	PASR / ASR / 2X refresh, ODTs
32 to 59	Reserved	0	0	0	0	0	0	0	0	00H	—
60	Module nominal height	0	0	0	0	1	1	1	1	0FH	29 < height ≤ 30mm
61	Module maximum thickness	0	0	0	1	0	0	0	1	11H	
62	Reference raw card used	0	0	0	0	0	0	1	0	02H	Raw Card C
63	Address mapping from edge connector to DRAM	0	0	0	0	0	0	0	0	00H	0 = standard
64 to 116	Module specific section	0	0	0	0	0	0	0	0	00H	—
117	Module ID: manufacturer's JEDEC ID code, LSB	0	0	0	0	0	0	1	0	02H	Elpida Memory
118	Module ID: manufacturer's JEDEC ID code, MSB	1	1	1	1	1	1	1	0	FEH	Elpida Memory
119	Module ID: manufacturing location	x	x	x	x	x	x	x	x	xx	
120	Module ID: manufacturing date	x	x	x	x	x	x	x	x	xx	Year code (BCD)
121	Module ID: manufacturing date	x	x	x	x	x	x	x	x	xx	Week code (BCD)
122 to 125	Module ID: module serial number	x	x	x	x	x	x	x	x	xx	
126	Cyclical redundancy code (CRC) -DG	0	0	0	1	0	0	0	1	11H	
	-DJ	1	1	1	0	0	1	1	0	E6H	
	-AC	0	1	0	0	1	0	0	1	49H	
	-AE	0	0	0	0	1	0	0	0	08H	
	-AG	0	1	1	0	1	0	1	1	6BH	
	-8A	0	1	0	1	1	1	0	0	5CH	
	-8C	0	1	0	1	0	0	1	1	53H	
	127	Cyclical redundancy code (CRC) -DG	0	1	1	1	1	1	0	0	7CH
-DJ		1	1	0	1	0	1	0	0	D4H	
-AC		0	0	1	0	1	0	1	1	2BH	
-AE		1	0	0	0	0	0	1	0	82H	
-AG		0	1	1	1	0	1	1	1	77H	
-8A		1	0	1	0	0	1	1	1	A7H	
-8C		0	1	0	1	0	1	1	0	56H	
128		Module part number	0	1	0	0	0	1	0	1	45H
129	Module part number	0	1	0	0	0	0	1	0	42H	B
130	Module part number	0	1	0	0	1	0	1	0	4AH	J
131	Module part number	0	0	1	1	0	1	0	1	35H	5
132	Module part number	0	0	1	1	0	0	0	1	31H	1
133	Module part number	0	1	0	1	0	1	0	1	55H	U
134	Module part number	0	1	0	0	0	1	0	1	45H	E
135	Module part number	0	0	1	1	0	1	1	0	36H	6
136	Module part number	0	1	0	0	0	0	1	0	42H	B
137	Module part number	0	1	0	0	0	0	0	1	41H	A
138	Module part number	0	1	0	1	0	0	1	1	53H	S
139	Module part number	0	1	0	0	0	0	0	1	41H	A

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
140	Module part number	0	0	1	0	1	1	0	1	2DH	—
141	Module part number -DG, -DJ	0	1	0	0	0	1	0	0	44H	D
	-AC, -AE, -AG	0	1	0	0	0	0	0	1	41H	A
	-8A, -8C	0	0	1	1	1	0	0	0	38H	8
142	Module part number -DG, -AG	0	1	0	0	0	1	1	1	47H	G
	-DJ	0	1	0	0	1	0	1	0	4AH	J
	-AC, -8C	0	1	0	0	0	0	1	1	43H	C
	-AE	0	1	0	0	0	1	0	1	45H	E
	-8A	0	1	0	0	0	0	0	1	41H	A
143	Module part number	0	0	1	0	1	1	0	1	2DH	—
144	Module part number	0	1	0	0	0	1	0	1	45H	E
145	Module part number	0	0	1	0	0	0	0	0	20H	(Space)
146	Module revision code	0	0	1	1	0	0	0	0	30H	Initial
147	Module revision code	0	0	1	0	0	0	0	0	20H	(Space)
148	SDRAM manufacturer's JEDEC ID code, LSB	×	×	×	×	×	×	×	×	×	×
149	SDRAM manufacturer's JEDEC ID code, MSB	×	×	×	×	×	×	×	×	×	×
150 to 175	Manufacturer's specific data	0	0	0	0	0	0	0	0	00H	
176 to 255	Open for customer use										

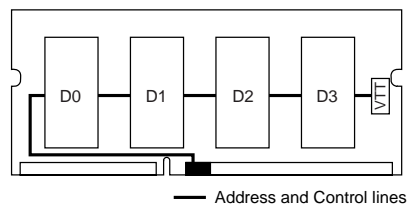
Block Diagram



Notes :

1. DQ wiring may be changed.
2. DQ, DQS, /DQS, ODT, DM, CKE, /CS relationships must be maintained as shown.
3. Refer to the appropriate clock wiring topology under the DIMM wiring details section of this document.

\* D0 to D3: 1G bits DDR3 SDRAM  
 Address, BA: A0 to A12, BA0 to BA2  
 Command: /RAS, /CAS, /WE  
 U1: 256 bytes EEPROM  
 Rs1: 15Ω  
 Rs2: 36Ω



## Electrical Specifications

- All voltages are referenced to VSS (GND).

### Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Notes
Power supply voltage	VDD	-0.4 to +1.975	V	1, 3, 4
Input voltage	VIN	-0.4 to +1.975	V	1, 4
Output voltage	VOUT	-0.4 to +1.975	V	1, 4
Reference voltage	VREFCA	-0.4 to $0.6 \times VDD$	V	3, 4
Reference voltage for DQ	VREFDQ	-0.4 to $0.6 \times VDDQ$	V	3, 4
Storage temperature	Tstg	-55 to +100	°C	1, 2, 4
Power dissipation	PD	4	W	
Short circuit output current	IOUT	50	mA	1, 4

- Notes: 1. Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage temperature is the case surface temperature on the center/top side of the DRAM.
3. VDD and VDDQ must be within 300mV of each other at all times; and VREF must be not greater than  $0.6 \times VDDQ$ , When VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.
4. DDR3 SDRAM component specification.

**Caution** Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

### Operating Temperature Condition

Parameter	Symbol	Rating	Unit	Notes
Operating case temperature	TC	0 to +95	°C	1, 2, 3

- Notes: 1. Operating temperature is the case surface temperature on the center/top side of the DRAM.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0°C to +85°C under all operating conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between +85°C and +95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
- Refresh commands must be doubled in frequency, therefore reducing the refresh interval tREFI to 3.9µs. (This double refresh requirement may not apply for some devices.)
  - If Self-refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 bit [A6, A7] = [0, 1]) or enable the optional Auto Self-Refresh mode (MR2 bit [A6, A7] = [1, 0]).

**Recommended DC Operating Conditions (TC = 0°C to +85°C)**

**(DDR3 SDRAM Component Specification)**

Parameter	Symbol	min.	typ.	max.	Unit	Notes
Supply voltage	VDD, VDDQ	1.425	1.5	1.575	V	1, 2
	VSS	0	0	0	V	
	VDDSPD	3.0	3.3	3.6	V	
Input reference voltage	VREFCA (DC)	$0.49 \times VDDQ$	$0.50 \times VDDQ$	$0.51 \times VDDQ$	V	3, 4
Input reference voltage for DQ	VREFDQ (DC)	$0.49 \times VDDQ$	$0.50 \times VDDQ$	$0.51 \times VDDQ$	V	3, 4
Termination voltage	VTT	$VDDQ/2 - TBD$	TBD	$VDDQ/2 + TBD$	V	

Notes: 1. Under all conditions VDDQ must be less than or equal to VDD.

2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.

3. The AC peak noise on VREF may not allow VREF to deviate from VREF(DC) by more than  $\pm 1\%$  VDD (for reference: approx  $\pm 15$  mV).

4. For reference: approx.  $VDD/2 \pm 15$  mV.

**DC Characteristics 1 (TC = 0°C to +85°C, VDD = 1.5V ± 0.075V, VSS = 0V)**

Parameter	Symbol	Data rate (Mbps)	max.	Unit	Notes
Operating current (ACT-PRE)	IDD0	1333	560	mA	
		1066	520		
		800	460		
Operating current (ACT-READ-PRE)	IDD1	1333	680	mA	
		1066	620		
		800	560		
Precharge power-down standby current	IDD2PF	1333	160	mA	Fast PD Exit
		1066	140		
		800	120		
	IDD2PS	1333	56	mA	Slow PD Exit
		1066	52		
		800	48		
Precharge quiet standby current	IDD2Q	1333	280	mA	
		1066	240		
		800	200		
Precharge standby current	IDD2N	1333	300	mA	
		1066	260		
		800	220		
Active power-down current (Always fast exit)	IDD3P	1333	180	mA	
		1066	160		
		800	140		
Active standby current	IDD3N	1333	380	mA	
		1066	340		
		800	300		
Operating current (Burst read operating)	IDD4R	1333	1160	mA	
		1066	920		
		800	720		
Operating current (Burst write operating)	IDD4W	1333	1320	mA	
		1066	1080		
		800	880		
Burst refresh current	IDD5B	1333	1340	mA	
		1066	1260		
		800	1180		
All bank interleave read current	IDD7R	1333	1520	mA	
		1066	1320		
		800	1260		

**Self-Refresh Current (TC = 0°C to +85°C, VDD = 1.5V ± 0.075V)**

Parameter	Symbol	max.	Unit	Notes
Self-refresh current normal temperature range	IDD6	40	mA	
Self-refresh current extended temperature range	IDD6ET	72	mA	
Auto self-refresh current	IDD6TC	72	mA	

**AC Timing for IDD Test Conditions**

For purposes of IDD testing, the following parameters are to be utilized.

Parameter	DDR3-1333		DDR3-1066		DDR3-800			Unit
	8-8-8	9-9-9	6-6-6	7-7-7	8-8-8	5-5-5	6-6-6	
CL (IDD)	8	9	6	7	8	5	6	tCK
tCK min.(IDD)	1.5	1.5	1.875	1.875	1.875	2.5	2.5	ns
tRCD min. (IDD)	12	13.5	11.25	13.13	15	12.5	15	ns
tRC min. (IDD)	48	49.5	48.75	50.63	52.50	50	52.5	ns
tRAS min.(IDD)	36	36	37.5	37.5	37.5	37.5	37.5	ns
tRP min. (IDD)	12	13.5	11.25	13.13	15	12.5	15	ns
tFAW (IDD)-×16	45	45	50	50	50	50	50	ns
tRRD (IDD)-×16	7.5	7.5	10	10	10	10	10	ns
tRFC (IDD)	110	110	110	110	110	110	110	ns

**DC Characteristics 2 (TC = 0°C to +85°C, VDD, VDDQ = 1.5V ± 0.075V)**

**(DDR3 SDRAM Component Specification)**

Parameter	Symbol	Value	Unit	Notes
Input leakage current	ILI	TBD	μA	VDD ≥ VIN ≥ VSS
Output leakage current	ILO	TBD	μA	DDQ ≥ VOUT ≥ VSS

**Pin Functions**

**CK, /CK (input pin)**

CK and /CK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of /CK. Output (read) data is referenced to the crossings of CK and /CK (both directions of crossing).

**/CS (input pin)**

All commands are masked when /CS is registered high. /CS provides for external rank selection on systems with multiple ranks. /CS is considered part of the command code.

**/RAS, /CAS, and /WE (input pins)**

/RAS, /CAS and /WE (along with /CS) define the command being entered.

**A0 to A12 (input pins)**

Provided the row address for active commands and the column address for read/write commands to select one location out of the memory array in the respective bank. (A10(AP) and A12(/BC) have additional functions, see below) The address inputs also provide the op-code during mode register set commands.

**[Address Pins Table]**

Address (A0 to A12)

Row address (RA)	Column address (CA)	Notes
AX0 to AX12	AY0 to AY9	

**A10(AP) (input pin)**

A10 is sampled during read/write commands to determine whether auto-precharge should be performed to the accessed bank after the read/write operation. (high: auto-precharge; low: no auto-precharge)

A10 is sampled during a precharge command to determine whether the precharge applies to one bank (A10 = low) or all banks (A10 = high). If only one bank is to be precharged, the bank is selected by bank addresses (BA).

**A12 (/BC) (input pin)**

A12 is sampled during read and write commands to determine if burst chop (on-the-fly) will be performed.

(A12 = high: no burst chop, A12 = low: burst chopped.)

**BA0 to BA2 (input pins)**

BA0, BA1 and BA2 define to which bank an active, read, write or precharge command is being applied. BA0 and BA1 also determine if a mode register is to be accessed during a MRS cycle.

**[Bank Select Signal Table]**

	BA0	BA1	BA2
Bank 0	L	L	L
Bank 1	H	L	L
Bank 2	L	H	L
Bank 3	H	H	L
Bank 4	L	L	H
Bank 5	H	L	H
Bank 6	L	H	H
Bank 7	H	H	H

Remark: H: VIH. L: VIL.

**CKE (input pin)**

CKE high activates, and CKE low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE low provides precharge power-down and self-refresh operation (all banks idle), or active power-down (row active in any bank). CKE is asynchronous for self-refresh exit. After VREF has become stable during the power-on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper self-refresh entry and exit, VREF must be maintained to this input. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, /CK, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self-refresh.

**DQ (input and output pins)**

Bi-directional data bus.

**DQS and /DQS (input and output pin)**

Output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS is paired with differential signals /DQS to provide differential pair signaling to the system during READs and WRITEs.

**ODT (input pins)**

ODT (registered high) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to each DQ, DQS, /DQS, DM. The ODT pin will be ignored if the mode register (MR1) is programmed to disable ODT.

**DM (input pins)**

DM is the reference signal of the data input mask function. DMs are sampled at the cross point of DQS and /DQS.

**VDD (power supply pins)**

1.5V is applied. (VDD is for the internal circuit.)

**VDDSPD (power supply pin)**

3.3V is applied (For serial EEPROM).

**VSS (power supply pin)**

Ground is connected.

**VTT (power supply pin)**

I/O termination supply for SDRAM.

**VREFDQ (power supply)**

Reference voltage for DQ.

**VREFCA (power supply)**

Reference voltage for CA.

**/RESET (input pin)**

/RESET is negative active signal (active low) and is referred to GND.

**/EVENT (output pin)**

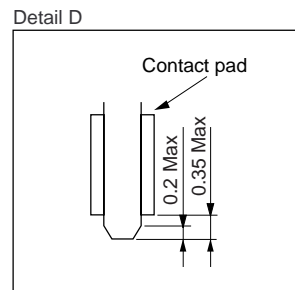
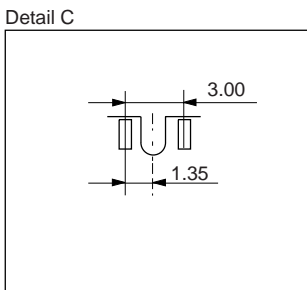
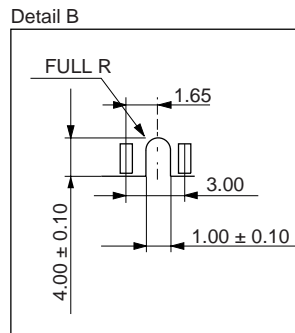
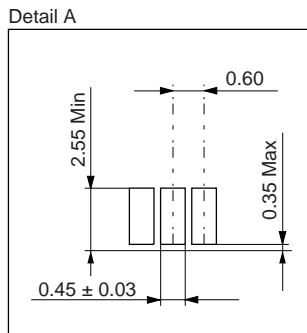
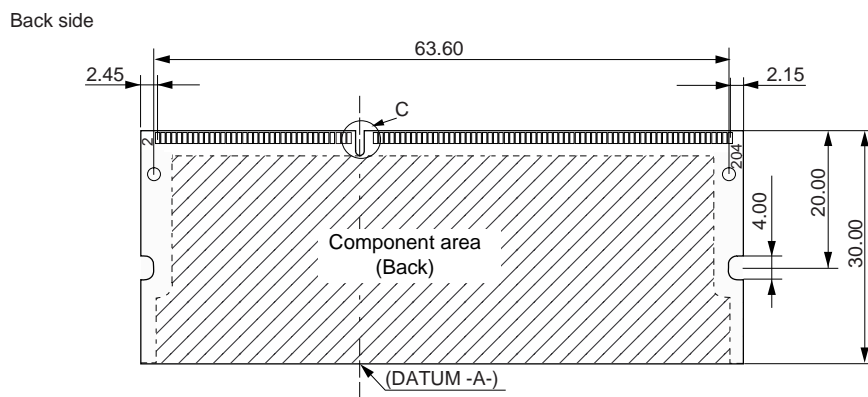
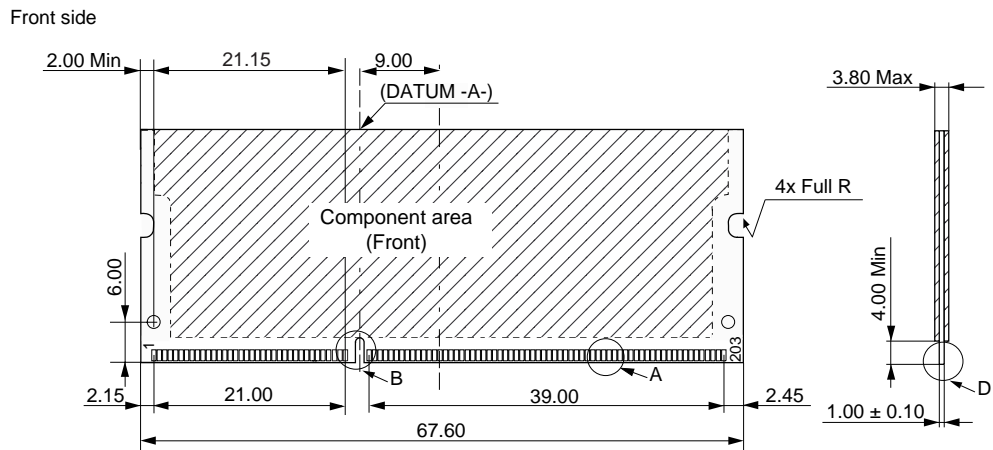
The /EVENT pin is reserved for use to flag critical module temperature. A resistor may be connected from /EVENT bus line to VDDSPD on the system planar to act as a pull-up.

**Detailed Operation Part, Electrical Characteristics and Timing Waveforms**

Refer to the EDJ1104BASE, EDJ1108BASE, EDJ1116BASE datasheet (E1128E).

Physical Outline

Unit: mm



ECA-TS2-0215-01

**CAUTION FOR HANDLING MEMORY MODULES**

When handling or inserting memory modules, be sure not to touch any components on the modules, such as the memory ICs, chip capacitors and chip resistors. It is necessary to avoid undue mechanical stress on these components to prevent damaging them.

In particular, do not push module cover or drop the modules in order to protect from mechanical defects, which would be electrical defects.

When re-packing memory modules, be sure the modules are not touching each other.

Modules in contact with other modules may cause excessive mechanical stress, which may damage the modules.

MDE0202

**NOTES FOR CMOS DEVICES****① PRECAUTION AGAINST ESD FOR MOS DEVICES**

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

**② HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES**

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

**③ STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

CME0107

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- 1) Usage in liquids, including water, oils, chemicals and organic solvents.
- 2) Usage in exposure to direct sunlight or the outdoors, or in dusty places.
- 3) Usage involving exposure to significant amounts of corrosive gas, including sea air, CL<sub>2</sub>, H<sub>2</sub>S, NH<sub>3</sub>, SO<sub>2</sub>, and NO<sub>x</sub>.
- 4) Usage in environments with static electricity, or strong electromagnetic waves or radiation.
- 5) Usage in places where dew forms.
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